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Notice to Authors: Address all papers and editorial correspondence to J. P. Nash, 168 Engineering Research Laboratory, University of Illinois, Urbana, Ill. To avoid delay, 3 copies of papers and figures should be submitted, together with the originals of the figures which will be returned on request. All material will be returned if a paper is not accepted.

Change of Editorship

With the present issue, Ralph Meagher concludes his editorship of the TRANSACTIONS ON ELECTRONIC COMPUTERS, which he began in July, 1954, taking over from Werner Buchholz, who had edited this journal since its founding in 1952. The Professional Group on Electronic Computers has now grown to a total membership of 5300, and about 6300 copies of each issue of the TRANSACTIONS are printed. The Publication Committee believes that the post of Editor is one which should be changed about every two years so that readers may benefit from more than one point of view and so that the responsibility, which takes a considerable amount of time, will not remain with one person for too long an interval.

The PGEC is much indebted to Professor Meagher for the careful job he has done and for the many improvements he has made in the TRANSACTIONS and in the editorial functions of the PGEC. We are fortunate in being able to retain him as a member of the Editorial Board, a group headed by the Editor, which is intended to represent a cross section of the membership in matters of editorial policy.

The PGEC is also fortunate in having John P. Nash, Research Professor of Applied Mathematics at the Digital Computer Laboratory of the University of Illinois, as Professor Meagher's successor. Dr. Nash received the B.A. degree in mathematics from the University of California in 1936 and the Ph.D. degree in mathematics from the Rice Institute in 1940.

Dr. Nash has held the positions of instructor of mathematics at Notre Dame during 1940–41, research physicist at the Kimberly-Clark Corporation during 1945–50, and since 1950, positions with the Digital Computer Laboratory of the University of Illinois. During the war Dr. Nash was a member of the staff of the Radiation Laboratory at M.I.T., where he was responsible for important research on the cross sections of radar targets and the use of radar by both the Army and the Navy. He served as a scientific consultant to the Pacific Army Headquarters as a part of this war work.

Dr. Nash is responsible for much of the design work of the ORDVAC and Illiac computers, including especially those sections of the control for arithmetic. He is the author of large sections of the *ORDVAC Manual* and *Illiac Programming*, as well as other papers in mathematics. He is an active participant in the teaching, research, and computation activities of the Digital Computer Laboratory.

Dr. Nash has served as chairman of the Program Committee for the Association for Computing Machinery since 1954.

I hope that the members of the PGEC will keep Professor Nash well supplied with papers. Some new topics on which papers will be welcomed are: automatic translation, self-repairing machines, cryptographic applications of computers, new computers under construction, the marketing of computers, the design and utility of built-in checks, government agencies' computer programs, the need for bigger machines, pedagogical methods, the simulation of mental activity, self-reproducing machines, and machines outside the United States. It is hoped that lively discussions of some of these topics may shortly appear among the papers and Letters to the Editor in the TRANSACTIONS. Authors are reminded that they may secure more rapid publication by submitting their shorter papers for the Correspondence Section.

NELSON M. BLACHMAN, *Chairman*
Publication Committee

A New Type of Ferroelectric Shift Register*

JOHN R. ANDERSON†

Summary—**Ferroelectric shift registers having completely independent parallel or serial inputs and outputs have been designed and constructed. The principal components of these shift registers are single crystals of barium titanate and silicon junction diodes. Two ferroelectric units and two to three silicon junction diodes are required for each stage of the shift register. Practical operating speeds for 10-stage shift registers with transistor drives are at present from 0 to 5 kc. The small size of the ferroelectric units and the low power consumption in this speed range make the ferroelectric shift register attractive for many digital circuit applications.**

CIRCUITS used for storing one or more computer words composed of a number of binary digits or bits are commonly called registers. Each of the bits stored in a register is contained in discrete cells or stages which have two possible stable states. When the binary digits in each stage of a register can be simultaneously moved forward or backward step by step under the control of shifting pulses without interfering with each other, we call the register a shift register. The shift register can perform four basic operations which are very useful in data processing fields such as digital computing and telephone switching. These basic operations are information storage, pulse counting, transferring information between systems of different pulse rates, and transferring information from serial form to parallel form or vice versa. The shift register therefore finds application in data processing for serial-to-parallel conversions, synchronous buffer storage, storage of data and orders, counting, checking, and sequencing.

Because of this wide field of possible use, shift registers have been fabricated from many components such as vacuum tubes, transistors, gas tubes, relays, and magnetic cores. Several years ago a shift register using ferroelectrics was designed and constructed to demonstrate the feasibility of barium titanate storage devices.[1] This paper describes a new type of ferroelectric shift register circuit which is extremely versatile in its operation and requires fewer diodes and ferroelectric crystal connections than did the first ferroelectric shift register.

Basic Ferroelectric Operation

The operation of the shift register is based upon the switching characteristics of two series-connected ferroelectric storage cells and the reverse saturation or avalanche break-down voltages of fused silicon alloy diodes.

Let us first review the switching and storage process in a ferroelectric. In Fig. 1 is illustrated a typical ferroelectric hysteresis loop with a 60-cps driving voltage for a good single crystal barium titanate ferroelectric device. A somewhat similar hysteresis loop is also obtained for crystals of guanidine aluminum sulphate hexahydrate.[2] The operating hysteresis loop under pulse conditions is shown in dashed lines. Let us assume that the stable 0 voltage state shown as point A represents the condition in which a binary "0" is stored. For this condition, all of the electric dipoles between the electrodes on the ferroelectric material are oriented as shown at the top left of Fig. 1.

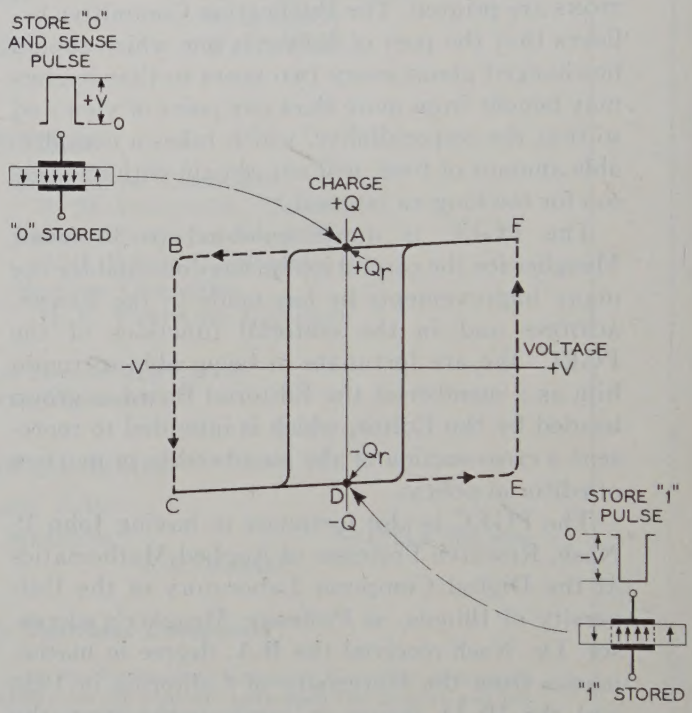

Fig. 1—Ferroelectric hysteresis loop and the orientation of permanent electric dipoles at the stable states.

The second stable state of the ferroelectric at point D on the hysteresis loop represents a binary "1," and the electric dipoles in the ferroelectric are oriented in the opposite sense from the binary "0" state as shown in the lower right of Fig. 1. If the ferroelectric is at point A and a negative voltage step with a very fast rise time (*i.e.*, <0.1 μs) is applied, the switching path A, B, C will be followed instead of the 60-cps hysteresis loop because the dipoles cannot switch instantaneously with

* Manuscript received by the PGEC, May 29, 1956; revised manuscript received, September 18, 1956.

† The National Cash Register Co., Dayton, Ohio. Formerly with Bell Telephone Labs., Inc., Murray Hill, N.J.

[1] J. R. Anderson, "Ferroelectric storage elements for digital computers and switching systems," *Elec. Eng.* vol. 71, pp. 916–922; October, 1952.

[2] A. N. Holden, B. T. Matthias, W. J. Merz, and J. P. Remeika, "A new class of ferroelectric crystals," *Phys. Rev.*, vol. 98, pp. 546; April 15, 1955.

the applied voltage. Therefore, only the normal displacement charge, characteristic of a capacitor, can flow from A to B. From point B to C, the change in charge is due to the dipoles switching. When the voltage step is removed, the state of the ferroelectric changes from C to D and again we have a small instantaneous change in charge similar to the displacement charge when a capacitor is discharged. The path D-E-F-A is followed when a positive voltage is applied to read out or "sense" a binary "1" and we again have three different changes in charge occurring of which only the change E-F represents dipoles switching. A binary "0" is read out or sensed by applying a positive voltage pulse and the path A-F-A is followed.

The changes in charge flowing to the ferroelectric crystal unit can most easily be detected by observing the current flowing through a series impedance as shown in Fig. 2, since $i = dq/dt$. The voltage pulses applied to

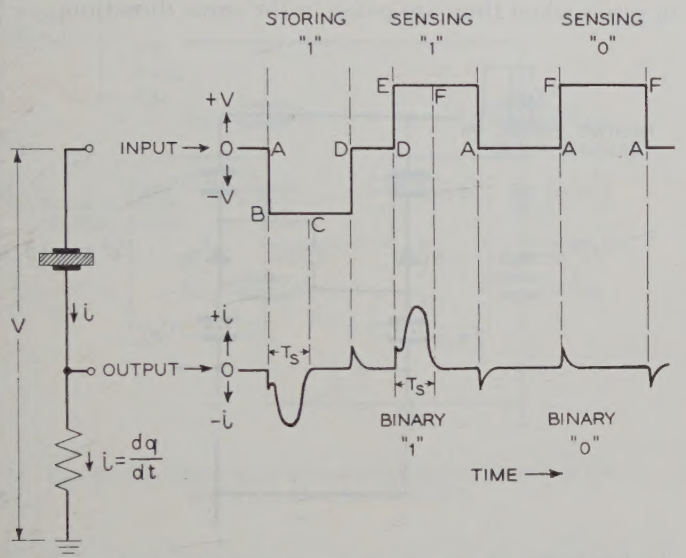

Fig. 2—Pulse response of a ferroelectric.

the ferroelectric during storage and sensing are shown at the right of the input terminal and have letters corresponding to the points on the operating hysteresis loop of Fig. 1. The current pulses through the load resistor due to the application of the voltage pulses are shown directly below. The length of the current pulse, T_s, is the switching time or total time required for reversing all dipoles between the electrodes.

Fig. 3 illustrates the nature of the switching characteristic. It shows a measured plot of the inverse switching time $1/T_s$ or peak current switched as a function of the voltage applied across the electrodes of an 0.002-inch thick barium titanate crystal. The $1/T_s$ function is linear for switching times below about 5 microseconds and at applied voltages above 10 volts. The amount of charge switched for a given unit is nearly constant regardless of the applied field. Therefore, the peak current switched is proportional to $1/T_s$ and is a linear function of applied voltage above 10 volts. For lower applied

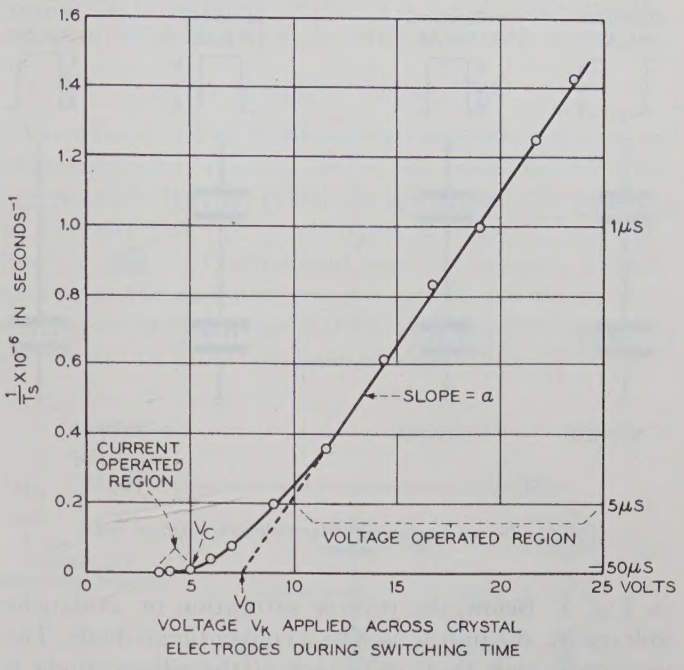

Fig. 3—Inverse switching time, $1/T_s$, as a function of applied voltage for an 0.002-inch thick barium titanate crystal.

voltages and longer switching times the current is no longer a linear function of applied voltage.

It has been proposed by Merz[3] and others that a ferroelectric crystal might be approximated by an equivalent resistance shunted by a small capacitance. This is a useful concept when studying some switching parameters, but it only approximates the crystal performance over a very small range of applied voltages.

Let us next examine the operation of two ferroelectric storage cells of identical characteristics connected in series as shown in Fig. 4(a). When the initial polarizations of both of the ferroelectrics are in a direction opposing the applied sensing voltage, they will both be switched by a sensing pulse. However, when the initial polarizations of the two ferroelectric crystals are opposing as shown in Fig. 4(b), neither of the crystals can be switched by applying voltages of either polarity. The following notation will be used in describing the state of the two-ferroelectric circuit. A binary "1" is stored or has just been sensed when the polarization of the two ferroelectrics is in the same direction while a binary "0" is stored when the polarizations are opposing as shown in Fig. 4(b). As shown there, the circuit equivalent for the binary "0" state is a small capacitor in series with the lower ferroelectric. The capacitor blocks the flow of switching current to the lower ferroelectric.

Gating by Silicon Alloy Diodes

Silicon alloy diodes are used for gating in the shift register. An idealized V-I characteristic for a typical silicon diode and the operating region used are shown

[3] W. J. Merz, "Domain formation and domain wall motions in ferroelectric $BaTiO_3$ single crystals," *Phys. Rev.*, vol. 95, pp. 690–698; August 1, 1954.

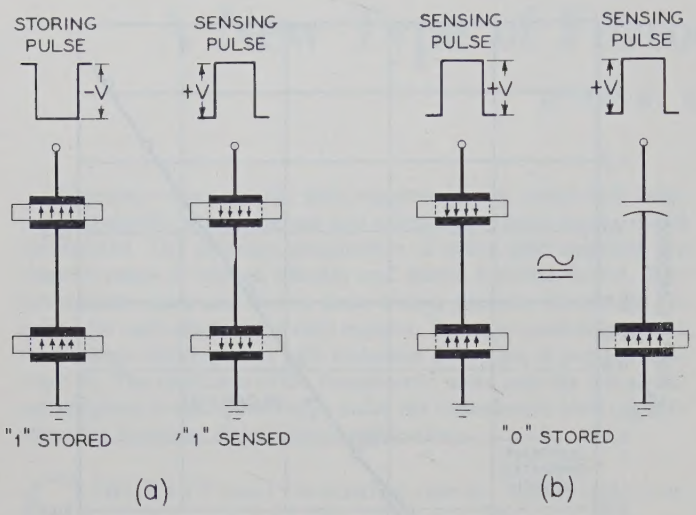

Fig. 4—Series operation of ferroelectric storage cells.

in Fig. 5. Below the reverse saturation or avalanche voltage S_n, the unit is used as a conventional diode. The extremely high back resistance of the silicon diode is necessary for proper operation of the ferroelectric shift register. However, since current requirements are relatively low for ferroelectrics, it is not necessary to have very high conduction in the forward direction. In general, a drop of 0.5 to 1 volt can be tolerated for forward currents of 20 ma or less and reverse currents below breakdown should be under 0.1 microampere.

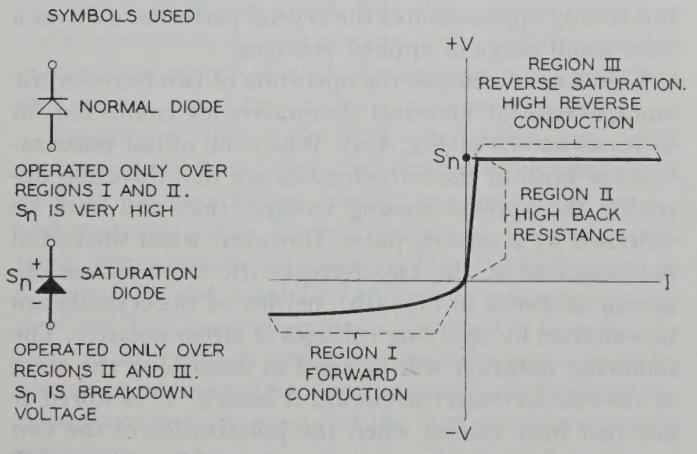

Fig. 5—Idealized characteristics of the silicon junction diode.

The reverse saturation or avalanche characteristic of the silicon diode is also extremely useful for gating. The diode acts essentially as an open circuit for all reverse voltages below the saturation point S_n of Fig. 5. As soon as the reverse voltage exceeds S_n, the diode acts as a closed circuit in series with a bias battery of S_n volts.

The current which the diode can carry in this reverse saturation region, of course, is limited by its maximum power dissipation. The present commercial diodes have an average power dissipation of about 125 mw. Diodes having saturation voltages ranging from 7 to 20 volts have been used in ferroelectric shift registers. Therefore, the average diode currents within the above power dissipation limit run from 6 to 18 ma at these breakdown voltages. The diode currents in shift registers built to date have run only from 0.1 to 4.0 milliamperes. Fig. 6 illustrates how the saturation characteristics of silicon diodes are used for gating ferroelectrics on positive power or sensing pulses. Ferroelectrics C_{s1}, C_{s2}, C_{s3}, and C_{s4} are initially polarized as shown by the dipole direction arrows on the crystals. Ferroelectrics C_{s1} and C_{s2} will be switched in series by the positive sensing pulse if its voltage is about three times the saturation voltage of S_1. Unit C_{s4} could also switch in series with C_{s1} as C_{s2} does were it not for the blocking of both saturation diodes S_1 and S_2 in series. However, S_2 will allow C_{s3} and C_{s4} to switch in series when they are initially poled in the same direction because saturation voltage S_2 is equal to S_1. Diode D_1, which does not use the saturation region, prevents any switching on positive pulses of C_{s3} and C_{s2} in series when they are poled in the same direction.

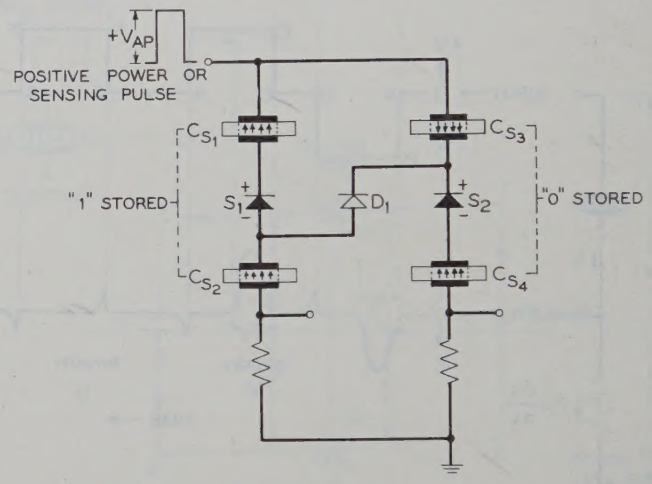

Fig. 6—Use of silicon diodes to gate positive ferroelectric switching pulses.

Fig. 7 illustrates how saturation diodes are used for gating on negative pulses. Ferroelectrics C_{s3} and C_{s2} can be switched in series on a negative pulse while C_{s1} is prevented from switching with C_{s2} by the saturation diode S_1. Likewise C_{s3} will switch completely through C_{s2} rather than trying to switch through C_{s4} because of the blocking of saturation diode S_2.

The blocking performed by saturation diodes S_1 and S_2 could just as well be accomplished with normal diodes. However, since double anode saturation diodes are commercially available, the functions performed by the circuits of Figs. 6 and 7 can be combined in a single circuit using one double anode diode in place of two separate diodes as shown in Fig. 8.

Silicon diodes are also used to perform another type of gating on setting or input pulses. This is illustrated in Fig. 9. In this figure, two input gates 1 and 2 have been added to the circuit of Fig. 8. Diode D_1 blocks positive pulses and saturation diode S_4 blocks negative

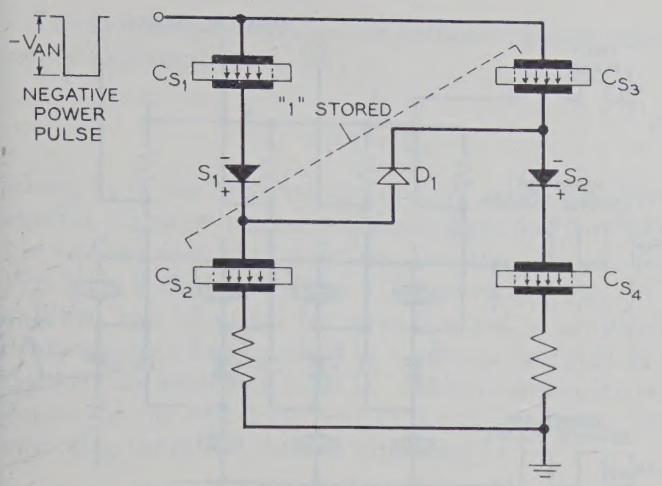

Fig. 7—Use of silicon diodes to gate negative ferroelectric switching pulses.

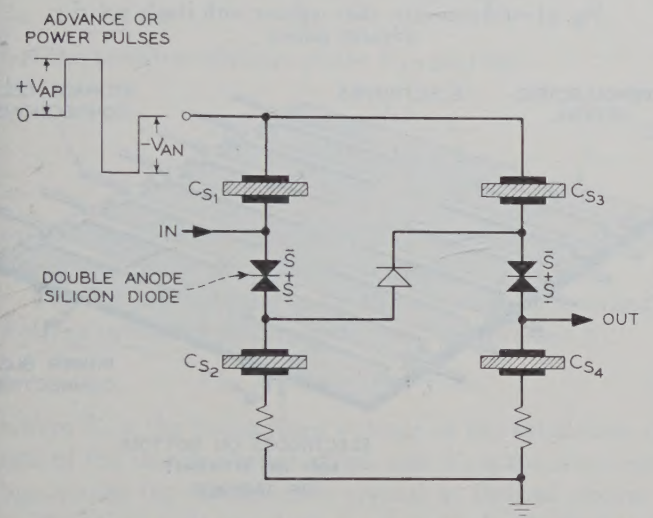

Fig. 8—Combination of silicon diode gating functions for positive and negative pulses.

pulses on the ferroelectric side of input 1. The ferroelectric circuit can then operate independently of the gate when no input pulses are applied. When a positive input pulse is applied at input 1 in coincidence with the negative power pulse, saturation diode S_4 is broken down and ferroelectric C_{s1} will be switched in the same direction as C_{s2} thus storing a binary "1" in the first stage.

A positive pulse applied at input 2 in coincidence with a negative power pulse will cause ferroelectric C_{s3} to switch in the same direction as C_{s4} thus storing a binary "1" in that stage. A double anode silicon diode is used for input 2. The S_2 section performs the same function as D_1 in input 1 while the S_3 section blocks from the input circuit any negative pulses across C_{s2}. Diode D_2 provides additional blocking for input 2 on positive pulses applied through ferroelectric C_{s3}. If input 2 were connected to point b instead of a, the double anode silicon diode would have to be replaced by the two diodes used on input 1 to prevent C_{s3} from switching back through the input on positive power pulses. This might occur because the breakdown voltage of S_2 is only high enough to prevent switching of C_{s1} in series with both S_1 and S_2.

Shift Register Operation

The circuit of Fig. 9 forms two complete stages of a ferroelectric shift register, and it has been expanded to four stages in Fig. 10. When the shift register is empty, the ferroelectrics will be polarized in opposing pairs as shown in Fig. 9. Positive and negative advance pulses applied to the common power bus will not be able to switch any of the ferroelectrics, and the shift register will remain in this state until storage takes place.

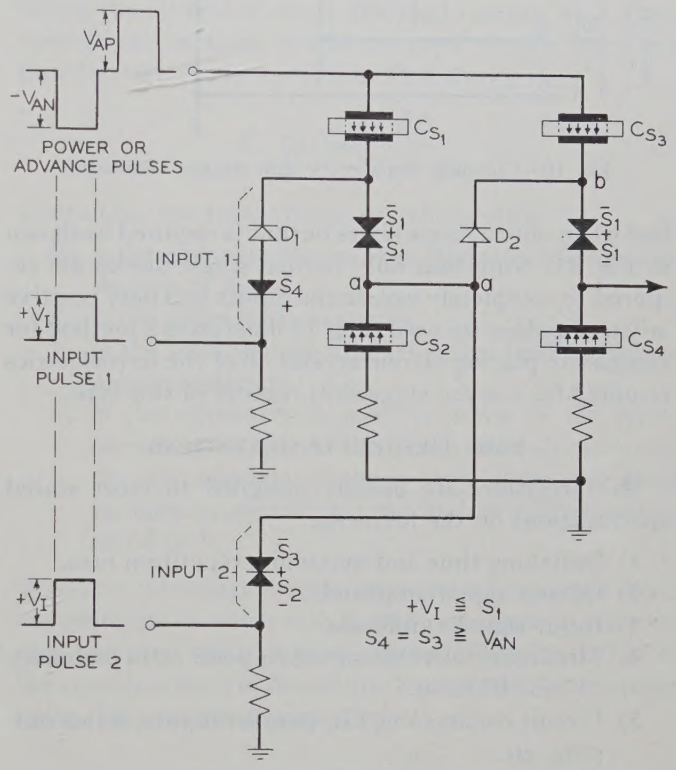

Fig. 9—Saturation diodes used to gate setting or storing pulses for ferroelectrics.

Binary "1"'s are stored or set in the shift register by reversing the polarity of selected upper ferroelectrics during the negative power pulse as explained above. One positive advance pulse followed by one negative advance pulse is then required to step the information one full stage. On the positive pulse ferroelectrics C_{s1} and C_{s2}, or C_{s3} and C_{s4} can be switched in series provided they are both poled in the same direction (binary "1" stored). On the negative advance pulses, ferroelectrics C_{s2} and C_{s3} can be switched in series. Thus information which has been stored on the parallel input can be stepped along in serial form to a single output load R_L as shown in Fig. 10. Alternatively, the input can be applied in serial form to a single input terminal such as 1 in Fig. 10, and it can then be stepped along and observed at parallel output loads R_0.

The shift register circuit can be considerably simpli-

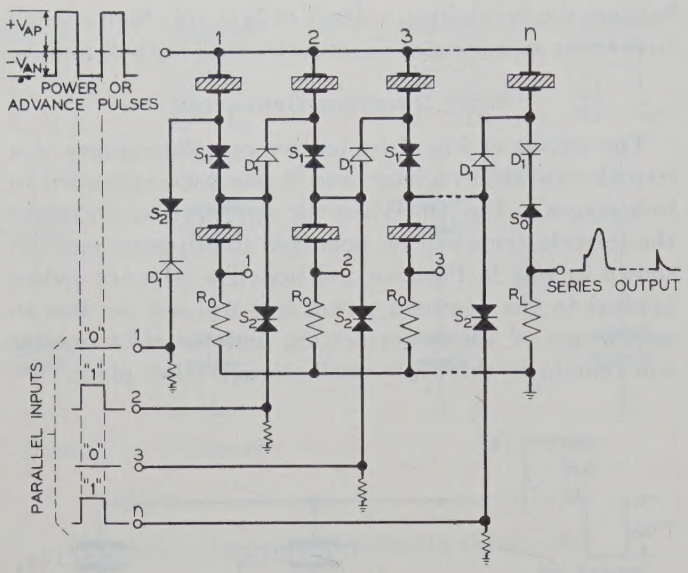

Fig. 10—Complete ferroelectric shift register schematic.

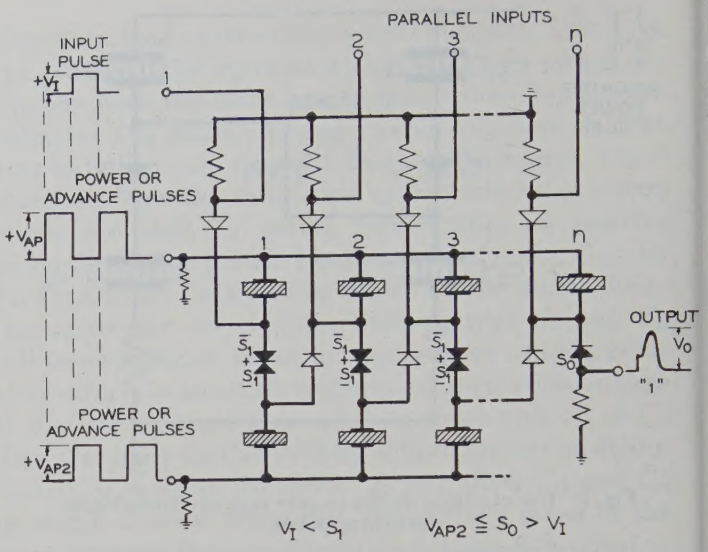

Fig. 11—Ferroelectric shift register with single polarity advance pulses.

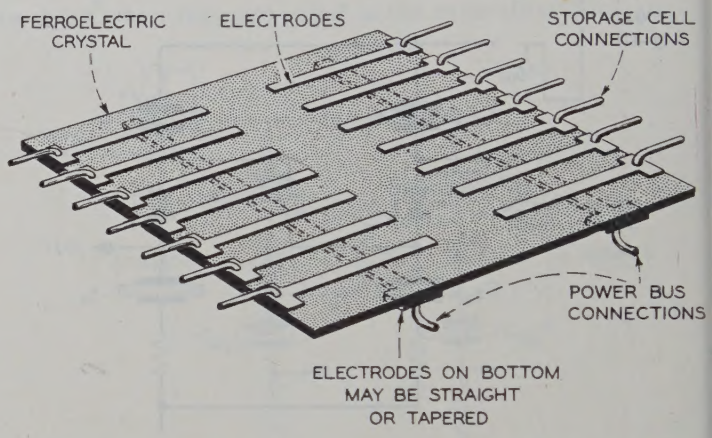

Fig. 12—Compact arrangement of shift register ferroelectric units for 7 stages.

fied when only a single series output is required as shown in Fig. 11. Note that only normal single diodes are required to completely isolate the inputs and only positive advance pulses are used. Fig. 12 illustrates a method for compactly placing on one crystal all of the ferroelectrics required for a seven stage shift register of this type.

Some Design Considerations

Shift registers are usually designed to meet stated specifications on the following:

1) Switching time and maximum repetition rate.
2) Output signal amplitude.
3) Input signal amplitude.
4) Minimum tolerable signal-to-noise ratio or binary "1" to "0" ratio.
5) Circuit connection; *i.e.*, parallel inputs, series outputs, etc.
6) Margins on driving voltages.

Items 1) to 4) above are determined primarily by the choice of ferroelectric material, the dimensions of the ferroelectric capacitor, the power or driving voltages used, and the saturation voltage of available diodes. Some typical examples and design limitations with barium titanate will be given below.

Maximum Repetition Rates, Switching Times, Input and Output Signal Amplitudes

The maximum repetition rate in barium titanate is determined mainly by internal heating due to the heat dissipation that occurs during switching. Practical upper limits at the present time appear to be about 100,000 pulses per second for units having electrodes 16×10^{-6} square inches in area. As the electrode size is increased, the upper frequency must be reduced. The largest units studied which have electrode areas of 440×10^{-6} square inches appear to have a safe upper frequency limit of about 10 kc. Improvements in unit fabrication and better provisions for heat dissipation might raise these limits considerably.

The switching time T_{2s}' for each shift register stage is a function of the switching time T_S of the ferroelectrics and the resistance R_L in series with the crystal. As was shown in Fig. 3, the inverse switching time $1/T_S$ of a ferroelectric is a linear function of applied voltage for voltages above about 10 volts across an 0.002-inch thick ferroelectric. This region is called the voltage operated region since the ferroelectric is ideally driven from a very low impedance source. The operating region around the 60-cps coercive voltage V_c has been called the current operated region since the ferroelectric presents a rather high impedance here and should be driven from a relatively high impedance source so that after switching is completed, the voltage across the ferroelectric can rise well above the coercive voltage to insure that the ferroelectric is completely switched. In the analysis which follows, calculations for switching time, input voltage, and output voltages are considered first for the constant voltage region and secondly for the constant current region.

The switching time T_s for the voltage operated region can be expressed by:

$$T_s = \frac{1}{\alpha(V_k - V_a)} \tag{1}$$

where V_k is the total voltage applied across the ferroelectric, V_a is the intercept of the straight line portion of the inverse switching function and the abscissa (see Fig. 3), α is the slope of the $1/T_s$ curve (see Fig. 3).

When two identical ferroelectrics and a saturation diode are switched in series in a voltage operated shift register, the switching time T_{2s}' of the combination will determine the switching time of the shift register. The switching times can then be expressed by:

$$T_{2s}' = \frac{1}{\alpha\left\{\frac{V_{AP} - S_1}{2} - V_a\right\}} \tag{2a}$$

for the positive advance pulse V_{AP} and by:

$$T_{2s}'' = \frac{1}{\alpha\left\{\frac{V_{AN}}{2} - V_a\right\}} \tag{2b}$$

on the negative advance pulse V_{AN} where S_1 is the breakdown voltage of the saturation diode.

The output voltage V_{0N} for the last stage of a constant voltage operated shift register can be expressed by:

$$V_{0N} = V_{AP} - (V_k + S_0) \tag{3}$$

where S_0 is the breakdown voltage of the saturation diode of the last or output stage, and V_k is the total voltage across the ferroelectric crystal as defined above.

Eq. (1) is used to calculate what V_k should be for the ferroelectrics used in the shift register in order to obtain the desired switching time.

The input signal to the ferroelectric shift register of Fig. 10 must be large enough to help the negative advance pulse break down the input saturation diodes S_2. This breakdown voltage S_2 must also be equal to or greater than the negative advance pulse voltage to insure that there is no possibility of switching or partially switching ferroelectrics through the input circuit. If we then assume that $S_2 \geqq V_{AN}$ where V_{AN} is the negative power or advance pulse, we can write for constant voltage operation:

$$|V_I| = S_2 + V_k - |V_{AN}|. \tag{4}$$

It is important that the amplitude of the input pulse V_I does not exceed $S_1 + S_2 - V_{AN}$ to insure that no ferroelectric in any stage beyond the input stage is switched by an input pulse. This means that the maximum value of V_k is limited to S_1 in the circuit of Fig. 10. In the shift register of Fig. 11 the input pulse is always equal to V_k since there is no drop in the input diode and no advance pulse is applied to the ferroelectric being set by the input pulse.

Barium titanate crystals of 0.002-inch thickness do not in general operate reliably at voltages below 10 volts except when driven from constant current sources. This means that while the crystal is switching, the applied switching pulse must be left on long enough to allow the voltage across the crystal to rise above 10 volts. This region of current operation is of considerable importance when output pulses 100 microseconds or more in length are desired. Constant current operation is simulated in the shift register by using a constant voltage drive and a high impedance in series with each of the ferroelectrics. For switching times of 100 microseconds or more, which occur in this current operated region, the switching time T_s' can be derived by calculating the current through the load resistor at a given voltage and relating this to the total charge which can flow through the ferroelectric. This then gives:

$$T_s' \cong Q_{SW}\frac{RL}{V_t - V_c} \tag{5}$$

where Q_{SW} the total charge switched $= 2Q_R$.

Q_R is the remanent charge of the ferroelectric hysteresis loop of Fig. 1.

R_L is the series load resistance.

V_t is the total voltage applied across load resistance and ferroelectric.

V_c is the approximate coercive force of the ferroelectric at 60 cps. At this point, the voltage across the ferroelectric changes very little for large changes in switching time and is approximately equal to V_c.

When two identical ferroelectrics and a saturation diode are switched in series with a load resistance in the current operated shift register, the switching time T_{2s}' of the combination will determine the length of the output pulse. This can be expressed by:

$$T_{2s}' \cong Q_{SW}\frac{R_L}{V_{AP} - (2V_c + S_1)} \tag{6a}$$

where S_1 is the breakdown voltage of the saturation diode, and V_{AP} is the positive advance pulse. The switching time T_{2s}'' on the negative advance pulse V_{AN} can be expressed by:

$$T_{2s}'' \cong Q_{SW}\frac{R_L}{V_{AN} - 2V_c}. \tag{6b}$$

The output voltage V_{0N} for the last stage of a constant current operated shift register will be of the same form as for the constant voltage case or:

$$V_{0N} = V_{AP} - (V_c + S_0) \tag{7}$$

where S_0 is the breakdown voltage of the saturation diode of the last stage. Likewise, the output voltage V_0 for any of the intermediate stages is given by:

$$V_0 = V_{AP} - (2V_c + S_1) \tag{8}$$

where S_1 is the breakdown voltage of the saturation

diodes used in all but the last stage. S_1 may be equal to S_0, but is generally chosen to be lower in value. Since the breakdown voltage S_1 must provide complete decoupling for successive stages, we can also write:

$$S_1 \geqq (V_0 + V_c) \text{ for constant current operation} \quad (9a)$$

or

$$S_1 \geqq (V_0 + V_k) \text{ for constant voltage operation.} \quad (9b)$$

The input signals to constant current operated ferroelectric shift registers must follow the same rules set down for the constant voltage operation except that V_c replaces V_k. Thus (4) for input voltage on the shift register of Fig. 10 becomes:

$$|V_I| = S_2 + V_c - |V_{AN}|. \quad (10)$$

Calculations of switching times for the region between 5 and 100 microseconds or between constant voltage and constant current operation can best be made by graphical methods.

Signal-to-Noise Ratios

The binary "1" to "0" ratios or signal-to-noise ratios of shift registers are determined by the ratios for individual crystals, crystal polarizations and electrode areas, the back impedance of the silicon diodes used in the shift register, and the control of input and advance pulse amplitudes.

If the input and advance pulses are kept within the limits defined by the formulas in the previous section, and electrode areas are properly proportioned, the "1" to "0" ratios will be determined entirely by the ferroelectric crystal unit signal-to-noise ratio when switching through a silicon diode and leakage through the back impedance of the silicon diodes. In the parallel input shift registers of Figs. 10 and 11, the electrode areas of all the upper crystal units should all be equal or graded in order, running from the smallest area for the first stage to the largest area for the nth stage. The electrode areas of the lower units need not be graded, but they should all be at least as large as the area for the nth stage unit. This will insure that all stages can switch completely through any succeeding stage. There will then be no unswitched portion of a stored binary "1" signal left in any crystal to reverse on the next positive advance pulse to enhance the "0" signal.

When only a single series input is used, only the first or input crystal unit need be selected for electrode area. Its electrode area should be smaller than the electrode area of any other unit in the shift register to insure that the "0" signal is not enhanced.

Current leakage through the back impedance of the silicon diodes could cause partial setting of crystals in stages either before or after the correct stage. This would both enhance the "0" signal and decrease the "1" signal for that stage. However, if leakage currents are held at or below 0.1 μa when diodes are in their blocking condition, the charge leakage that takes place even for periods as long as 1 millisecond will have negligible effects on the "1" to "0" ratios.

The binary "1" to "0" ratio for a barium titanate crystal unit is theoretically above 100. However, in practical units having very small electrodes, there is a considerable amount of fringing of the electric field beyond the electrodes. This effectively increases the small signal capacitance and thus the binary "0" signal above values predicted by theory. For example, units having electrode areas of 16×10^{-6} square inches normally have binary "1" to "0" ratios of 7:1 to 15:1; units with 64×10^{-6} square inches may have ratios as high as 30:1 or better and units of 440×10^{-6} square inches may give ratios of 50:1 or better.

When operating in a shift register, the ferroelectric crystals are always switched through a series silicon diode. This series diode does not reduce the binary "1" or signal pulse switched from the ferroelectric to the output load, but it has been found to materially reduce the binary "0" current pulse from individual ferroelectrics. The amount of reduction of the binary "0" pulse runs from a factor of 3 for the poorest (*i.e.*, lowest signal-to-noise ratio) 16×10^{-6} square inch electrode unit to a factor of 10 for some of the poorer 440×10^{-6} square inch units.

Thus, it can be concluded that the most important factors in determining signal-to-noise ratios in shift registers are the ratios of ferroelectric electrode areas and polarization and the back impedance of the silicon diodes used. Practical signal-to-noise ratios of 10:1 to 30:1 have been obtained with 10-stage shift registers.

Circuit Connections and Margins on Driving Voltages

Different types of circuit connections have been illustrated in Figs. 10 and 11. It is apparent that a single series input could be used in place of the parallel inputs of these circuits so that full conversion between a series input and parallel outputs or parallel inputs and a series output is possible. The parallel outputs of the shift register can be directly connected together without affecting series shifting down the register. A common input signal can also be fed simultaneously to several different stages through the parallel input connections.

The limits on variations in driving voltage such as the power or advance pulses and input pulses are determined by the ratio of breakdown voltage on the saturation diodes relative to the minimum voltage which can be applied across the ferroelectrics for stable switching. The range between minimum and maximum drive voltages for reliable operation will be increased as this ratio is increased. With proper design, variations of ± 50 per cent can be tolerated on input pulse amplitudes. The negative advance pulses, V_{AN}, must always be of sufficient amplitude to fully switch two ferroelectrics in series. They can exceed this minimum value by a large margin if the breakdown voltages in the reverse direction of the series diodes are high. The positive advance pulse voltage should be held within limits of about ± 10 per cent. This is because the margin is relatively small between an advance pulse voltage sufficient

to completely switch two ferroelectrics through a saturation diode and a voltage large enough to give partial switching through more than one stage. However, due to the low current requirements, this drive voltage can be regulated quite easily with a single breakdown diode and resistor combination.

Performance and Applications

Several models of the ferroelectric shift register have been constructed with barium titanate crystals approximately 0.002 inch thick. Electrode areas of 16×10^{-6}, 64×10^{-6}, 290×10^{-6}, and 440×10^{-6} square inches have been used in different shift registers. Operating speeds for completed shift registers have run only from 10 to 2000 pps. However, tests have been made which indicate that shift registers with units having electrode areas of 64×10^{-6} square inches or less might be operated up to 50 or 100 kc. In the latter case, constant voltage operation at switching times of less than 5 μs would be used.

The shift registers built to date have been designed for constant current operation at switching speeds of 50 μs to 500 μs. For a 500-μs switching time, the driving or shifting current with the largest electrode unit (440×10^{-6} square inches) is below 0.28 ma per stage. Saturation diodes having breakdown voltages from 7 to 20 volts have been used in different designs. The advance or power pulse voltages required have been 30 to 35 volts on the positive advance or power pulse and 20 volts on the negative advance pulse. Output signals as high as 12 volts can be easily obtained with input or setting pulses of only 10 volts. The power pulse sources for all of these shift registers have been completely transistorized.

Fig. 13 shows the series output pulses from a 10-stage parallel input ferroelectric shift register in which 290×10^{-6} square inch electrode units have been used and the pulse rate is 1000 pps.

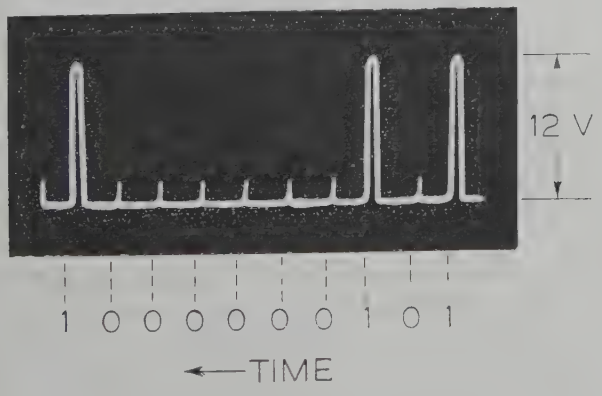

Fig. 13—Output pulses from a 10-stage ferroelectric shift register operating at 1000 pps. Barium titanate ferroelectric units with electrodes 290×10^{-6} square inches in area are used in the shift register.

It is apparent that the ratio between binary "1" and binary "0" pulses is quite good. The last pulse which has traveled completely through the shift register is only slightly smaller than the first pulse which has gone through only one stage.

It is interesting to note that the double anode silicon diode component of the shift register can be replaced by a small neon gas diode of the NE-2 variety. The gas diode has the advantages over the silicon diode of much lower cost and visual indication of operation. These are of course offset by the disadvantages of higher breakdown voltages of 70 to 100 volts and limited operating speed. A 10-stage ferroelectric shift register employing NE-2 diodes in place of the double anode silicon diodes has been successfully operated.

One of the primary difficulties with early barium titanate storage cells was that their electrical characteristics would gradually change almost as a function of the number of times the ferroelectrics were switched. More recently, due to improvements in ferroelectric materials and processing, some units have been obtained which exhibit only minor changes in characteristics even after hundreds of hours of operation. Under certain types of pulse operation, where voltages are not kept across the ferroelectric all the time (such as are encountered in matrix memories) these improved units do show a temporary drop in polarization during operation. However, this type of temporary instability is completely eliminated in shift register operation because there is no off-time between the applications of power or advance pulses.

The possible applications of the ferroelectric shift register cover data transmission and reception, decoding, counters, word generators, selective signaling and receiving, and small scale data storage. In applications where output pulses 100 μs or more long are required, the ferroelectric shift register can be used to advantage over the magnetic core shift register because driving currents for the ferroelectrics are very low and no auxiliary circuits are required to obtain long output pulses.

Conclusion

It has been shown that it is possible to construct ferroelectric shift registers having completely independent parallel or serial inputs and outputs or any combinations of these. Practical operating speeds may be from 0 to above 10,000 pps although the ferroelectric shift register is probably most useful at speeds below 2000 pps when very long output pulses are needed. The small size of the ferroelectric units, the low power consumption at low speeds, and completely transistorized drive circuits make the ferroelectric shift register attractive for many applications.

Acknowledgment

The author would like to acknowledge the contributions of the following people to this project. R. M. Wolfe designed and built the transistor driving circuits used for driving the first shift register models. R. V. Anderson, E. M. Walters, and R. W. Oman constructed several of the shift registers and made many tests on the ferroelectric units used in the registers. The author would like to thank A. W. Horton, Jr., W. J. Merz, and R. M. Wolfe for reviewing this manuscript and offering many valuable comments.

Junction Transistor Switching Circuits for High-Speed Digital Computer Applications*

G. J. PROM† AND R. L. CROSBY†

Summary—**This paper describes junction transistor switching circuits capable of reliable operation at a clock rate of one megacycle. These circuits, consisting of a flip-flop, a gated pulse amplifier, and diode gates, consume a minimum of power and operate over a temperature range of −55°C to +85°C with complete transistor interchangeability. Applications of these circuits to binary counters, shift registers, and accumulators are also presented.**

Introduction

HIGH-FREQUENCY junction transistors, introduced about two years ago, have made possible the design of reliable one-megacycle transistorized switching circuits. A paper by Wanlass[1] has emphasized the application of transistors to lower speed circuits. The circuits to be described here have been designed to obtain the fastest possible transient response from commercially available alloy junction transistors.

Rapid response in these switching circuits can be attained by several methods. Two of these methods are described by Linvill[2] and Beter.[3] This paper discusses another technique for the design of reliable high-speed germanium junction transistor switching circuits. These circuits consume a minimum of power, and operate over a wide ambient temperature range. The transistors used have a five-megacycle α cutoff frequency, are completely interchangeable, and are readily available in production quantities.

Transistor Characteristics

The grown junction germanium transistor was the first high-frequency type to become available. Although switching circuits can be designed around this transistor type, the alloy, diffusion, and surface-barrier transistors are more suitable for this application because they exhibit low and consistent values of extrinsic resistances. The extrinsic base resistance of r_b' and the extrinsic collector resistance r_c' limits the response time of the collector current to an increment of base voltage; a large value of r_c' limits the circuit efficiency and complicates the circuit design problem. Table I lists the transistor characteristics around which these circuits were designed. Since dissipations in excess of one or two milliwatts are seldom encountered in these applications, the collector dissipation rating is not important. Although a collector voltage rating of 20 volts is specified, the actual collector voltage never exceeds 12 volts. Note that maximum I_{c0} and minimum β are specified at the temperature extremes. These are the only temperature-dependent parameters that require design consideration. A liberal allowance for deterioration with time has been included in the values given for these transistor parameters. For example, a transistor with an initial β of 20 at 25°C is still suitable after a decrease in β of 40 per cent, allowing for an additional decrease of about 40 per cent which occurs between +25°C and −55°C. Many *p-n-p* and *n-p-n* transistor types are available which meet these requirements.

TABLE I

Required Transistor Characteristics

Maximum Ratings
Collector Voltage $V_c = 20$V
Junction Temperature $T_j = 85$°C

Parameter	Maximum	Minimum	Conditions
I_{c0} (ma)	.250	—	$V_c = 12$V $T = +85$°C
β (dc)	—	7	$I_e = 3$ ma $T = -55$°C $V_{ce} = 0.8$ V
F_{ca} (mc)	—	5	$V_c = 6$ V $I_e = 1$ ma
$r_{b'}$ (ohms)	200	—	—
$r_{e'}$ (ohms)	30	—	—

Since reliability was the most important factor in the design of these circuits, the lowest possible supply voltages were selected, consistent with the output requirements. The full load flip-flop output or enable voltage is about 5.5 volts, and the amplitude of the standard 0.3 microsecond pulse is 4.0 volts biased at −1.5 volts. These amplitudes are approximately double the minimum required drive levels. Although only three supply voltages are required, the circuits were designed to withstand voltage variations of at least ±40 per cent.

Other factors contributing to the operational reliability of these circuits are 20°C safety margins at both ends of the operating temperature range and the liberal use of emitter followers and transformer-coupled pulse amplifiers to provide proper impedance-matching.

Pulsed Diode Gate

A common gating requirement in a computer employing static logic is to detect coincidence between a flip-flop output and a train of clock pulses. Fig. 1 is a schematic diagram of a pulsed diode gate which performs this function. A high level (5.5 to 6.0 volts) from the

* Manuscript received by the PGEC, May 21, 1956; revised manuscript received September 4, 1956.

† Sylvania Elec. Products, Inc., Waltham Labs., Waltham, Mass.

[1] C. L. Wanlass, "Transistor circuitry for digital computers," IRE Trans., vol. EC-4, pp. 11–16; March, 1955.

[2] J. G. Linvill, "Nonsaturating pulse circuits using two-junction transistors," Proc. IRE, vol. 43, pp. 826–833; July, 1955.

[3] R. H. Beter, W. E. Bradley, R. B. Brown, and M. Rubinoff, "Direct coupled transistor circuit," *Electronics*, vol. 28, pp. 132–136; June, 1955.

flip-flop enables the gate, causing a current of about two milliamperes to flow through R_1, R_2, D_1, and the transformer secondary winding. Thus, diode D_1 is conducting, and D_2 is cut off. If a positive pulse is then applied across the transformer secondary winding, diode D_1 is cut off and D_2 conducts, allowing the gated current to flow in the load circuit. A low level (0.2 to 0.8 volt) from the flip-flop effectively removes the current supply, thereby disabling the gate.

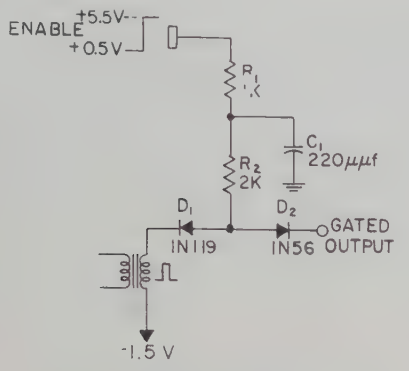

Fig. 1—Pulsed diode gate circuit.

The capacitor C_1 supplies the gate with a short memory so that the gating action is complete before flip-flop transients can effect the result.

The transformer secondary winding may be common to many gating and pulse amplifier circuits as long as the dc voltage drop across the winding does not approach 1.5 volts.

A desirable feature of this gating circuit is that it is relatively insensitive to input pulse level variations. Assuming a constant enable voltage, any input pulse amplitude greater than two volts will result in a constant output current.

Gated Pulse Amplifier

The gated pulse amplifier shown in Fig. 2 is a modification of the pulsed diode gate cirucit. The output diode has been replaced by a transistor amplifier so that a total current gain of about ten results. By increasing the gated input current to three milliamperes, an output current of 30 milliamperes is made available. The purpose of diode D_1 is to prevent transistor saturation and thereby limit pulse stretching. In the enabled condition the gated pulse amplifier consumes about 20 milliwatts of power; in the disabled condition it consumes about one milliwatt.

DC Gates

The gating of flip-flop levels requires a slightly different technique. Fig. 3(a) is a schematic of the dc *and* gating circuit, which can be used to gate two or more flip-flop outputs. If a low level appears at any input, the appropriate diode conducts, holding the output low. However, if all inputs are high, the *and* condition is

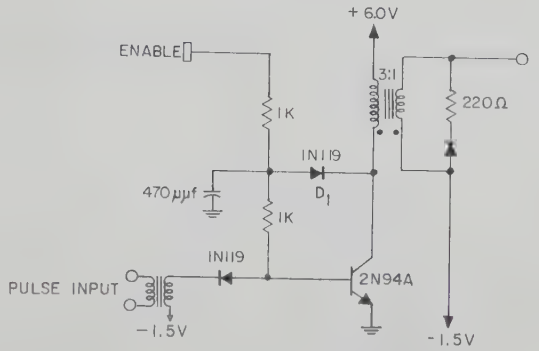

Fig. 2—Gated pulse amplifier circuit.

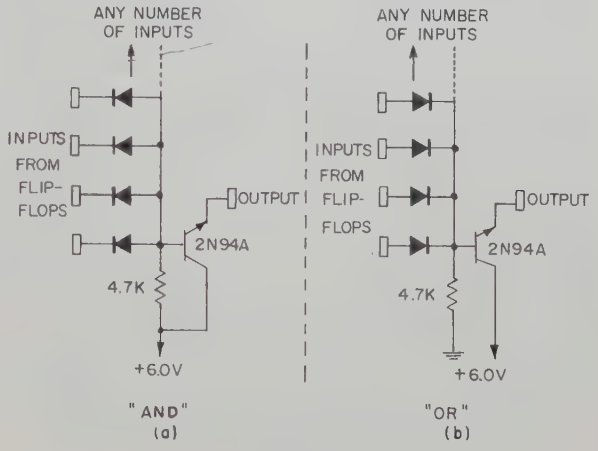

Fig. 3—DC gating circuits.

satisfied and the output is high. The dc *or* gate is shown in Fig. 3(b). If any or all of the inputs are high, the appropriate diodes conduct, resulting in a high level at the output. Emitter followers are usually required at the output to reduce loading of the gates.

Flip-Flop Circuit

Fig. 4 is a schematic diagram of the flip-flop circuit. The portion of the circuit indicated by the heavy lines is the familiar Eccles-Jordan configuration. Diodes D_1 and D_2 hold the collector at about 0.5 volt when the respective transistor is conducting. For the transistor types under consideration, this voltage is ample to hold the transistor out of saturation and thereby eliminate carrier storage effects. The emitter followers T_3 and T_4 act as impedance transformers to isolate the flip-flop transistors from loading effects of the cross-coupling network and external circuits. As a result, switching is rapid, and an output enable voltage is obtained which is nearly equal to V_{cc}. The *p-n-p* emitter followers T_5 and T_6 are only required when the dc *and* gating circuit (previously described) is being driven. A negative drive current is then supplied by T_5 and T_6 and the load capacitance is discharged by T_3 and T_4. If the load consists only of pulsed diode gates, gated pulse amplifiers, or dc *or* gating circuits, transistors T_5 and T_6 can be replaced by the diodes indicated by the dotted lines on the sche-

matic diagram (Fig. 4). In this case T_3 and T_4 supply the drive currents and the load capacitance is discharged by D_3 and D_4.

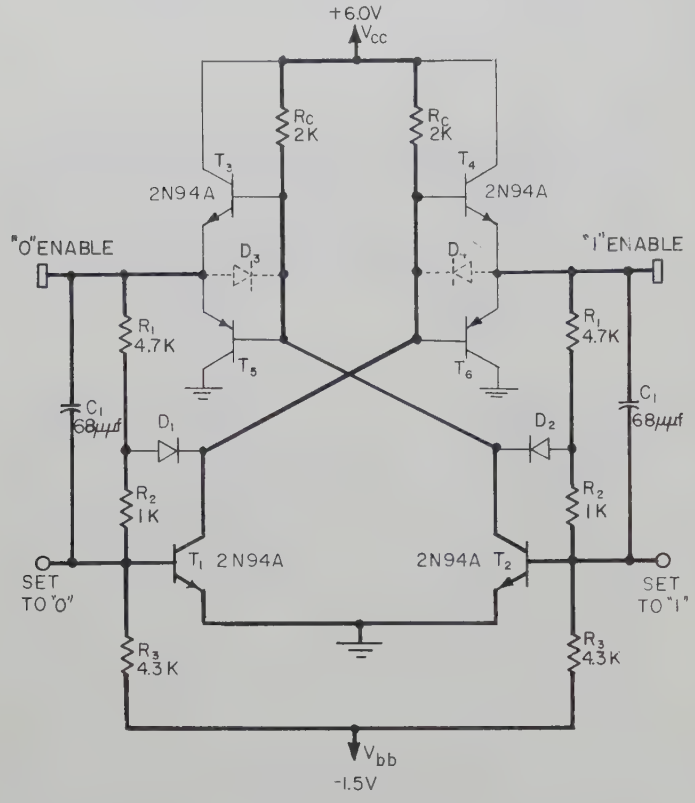

Fig. 4—Flip-flop circuit. Heavy lines indicate the familiar Eccles-Jordan circuit.

The component values for the flip-flop circuit were chosen so that reliable operation is obtained between the temperature range of -55°C and $+85$°C and at rates in excess of one megacycle. The supply voltages were chosen to provide the required bias currents and output voltages. R_c and C_1 were determined experimentally by adjusting them to the value which produced the desired rise and fall time.

The values of R_1, R_2 and R_3 were chosen to provide dc stability over the temperature range of -55°C to $+85$°C. At low temperatures I_{c0} is so small that it may be neglected. Since the magnitude of the dc β decreases with decreasing temperature, sufficient positive base current must be provided to hold the conducting transistor "on". At high temperatures, the "on" drive is no problem as a result of the increase of both the βI_b and the I_{c0} components of collector current. I_{c0} increases to very large values however, and sufficient negative base current must be provided to hold the "off" transistor collector current to a minimum. Thus two equations for base current may be set up. One of these equations is an expression for the base current of the conducting transistor at the lowest ambient temperature; the other is an expression for the base current of the cut-off transistor at the highest ambient temperature.

Let:[4]

$$A = V_{cc} - \frac{I_L R_c}{1+\beta} - 0.4 \qquad E = 0.5 \text{ volt}$$

$$B = V_{bb} + 0.2 \qquad F = I_{c0}$$

$$C = \frac{V_{cc} - 0.8}{\beta R_c} \qquad G = 0.8 \text{ volt}$$

$$D = V_{bb} - 0.1$$

where:

β = minimum dc grounded emitter current gain at the lowest ambient temperature.
I_L = maximum external load current.
I_{c0} = maximum cut-off current at the highest ambient temperature.

Then the following approximate equations for the two base currents may be set up:

$$I_{b(on)} = C = \frac{A}{R_1 + R_2} - \frac{B}{R_3}$$

$$I_{b(off)} = F = \frac{-E}{R_1 + R_2} + \frac{D}{R_3}.$$

A third equation expressing the voltage drop across R_2 is also required:

$$G = A - \frac{AR_1}{R_1 + R_2}.$$

Simultaneous solution of these equations results in the following expressions for R_1, R_2 and R_3:

$$R_1 = \frac{AD - BE}{CD + BF}\left(\frac{A - G}{A}\right)$$

$$R_2 = \frac{AD - BE}{CD + BF}\left(\frac{G}{A}\right)$$

$$R_3 = \frac{AD - BE}{CE + AF}.$$

Some of the approximations used in determining these equations are:

1) At low temperatures the voltage drop between base and emitter of the conducting transistor is about 0.2 volt.
2) At high temperatures a negative base current approximately equal to I_{c0} and a negative base voltage of about 0.1 volt will hold the collector current of the cut-off transistor at a minimum.
3) The external load current is much larger than the current flowing through R_1. If this is not true, the current drawn by R_1 must be estimated and added to the load current.

Although these equations are only approximate relationships, they are sufficiently accurate to provide useful design value. The values shown in Fig. 4 were calculated using the transistor characteristics given in Table I and assuming a load current of 5 milliamperes.

[4] In these equations, all voltage and current terms represent absolute magnitude.

With a two-milliampere trigger current, the rise time of collector voltage (turn-off time) is about 0.3 microsecond, and the fall time is about 0.2 microsecond. The output voltages are approximately 0.5 volt for the conducting transistor and 5.5 volts for the cut-off transistor under full load conditions. Each flip-flop output will supply five or six milliamperes of load current to gating circuits. If additional gating current is required, external emitter followers must be added. The unloaded flip-flop consumes about 25 milliwatts of power.

Pulse Amplifier

The pulse amplifier shown in Fig. 5 was designed to supply an output current of about 60 milliamperes. A current of this magnitude is often required when a large number of flip-flops and gates must be driven by a single source. Again note that the input transformer may be common to many circuits; in fact it may be the output transformer of a gated pulse amplifier or another pulse amplifier.

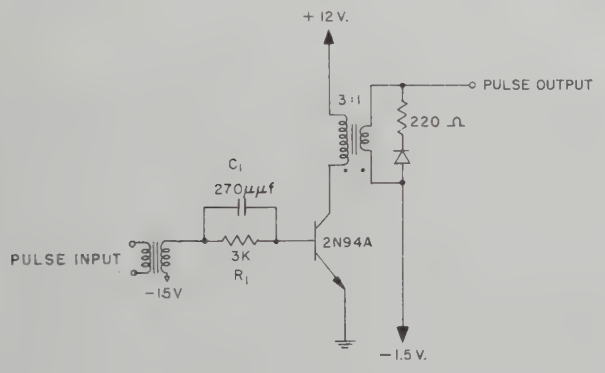

Fig. 5—Pulse amplifier circuit.

The capacitor C_1 provides a large initial surge of base current which results in a rapid rise of collector current. After the capacitor charges, the drive current is limited by the resistor R_1 such that carrier storage effects are minimized. The discharge of the capacitor at the end of the pulse period promotes rapid recovery of the transistor. Most of the power consumed by the pulse amplifier is pulse power.

Shift Register

Fig. 6 is a block diagram of a typical shift register. Initially the register is set at zero through diodes connected to the "zero" input of each flip-flop. Binary information is then inserted in parallel by means of read-in gates which set the appropriate stages to "1." Each shift pulse then shifts each bit one stage. Read-out is accomplished by parallel gating from the "1" side of each flip-flop. For reliable operation, a read-in or read-out pulse must be separated from a shift pulse by at least one microsecond. If the output is used only to set the flip-flops previously described, all of the gating can be done with pulsed diode gates.

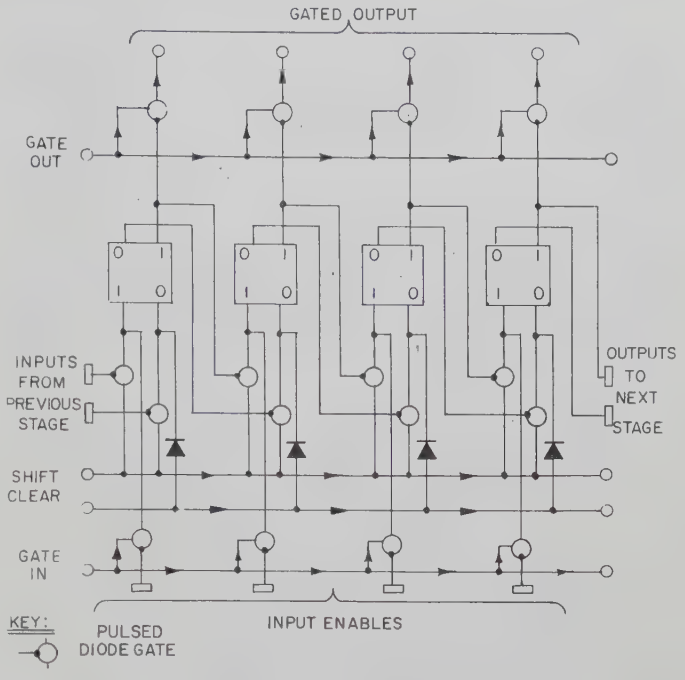

Fig. 6—Shift register.

Binary Counters

One possible binary counter configuration is shown in block diagram form in Fig. 7. Two pulsed diode gates on each flip-flop provide complement operation, and a gated amplifier transmits the carry pulse to the succeeding stage. Since the delay through the pulse amplifier is about 0.1 microsecond, only a few stages may be cascaded if timing between the first and last stages is important and if the counter is being operated at pulse repetition rates near one megacycle.

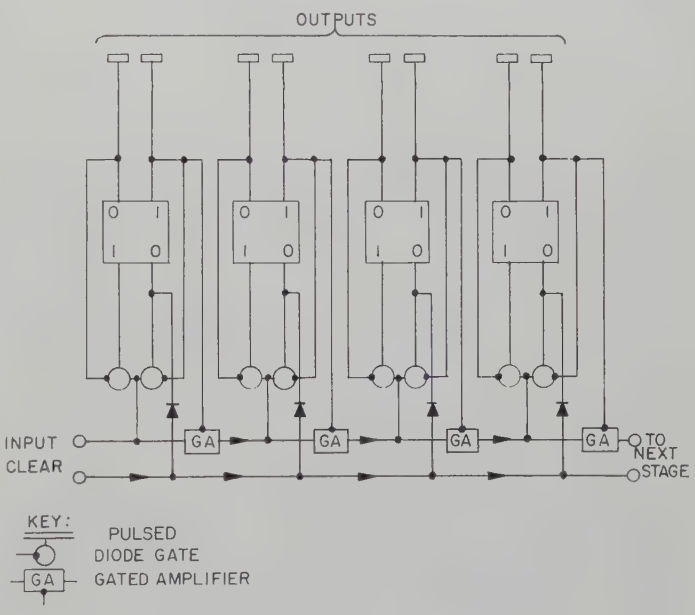

Fig. 7—Binary counter (Type 1).

Larger counters can be constructed using the technique shown in Fig. 8. Here dc *and* gates determine the carry conditions making simultaneous triggering of all flip-flops possible. The number of cascaded stages is limited to about four, since the *and* gates on succeeding stages would require a very large number of diodes. However, a twelve-stage counter, for example, might be broken up into three groups of four stages, with a gated "carry" amplifier between each group. The delay between the first and twelfth stage would then be only about 0.2 microsecond, as compared to 1.1 microseconds for the other configuration.

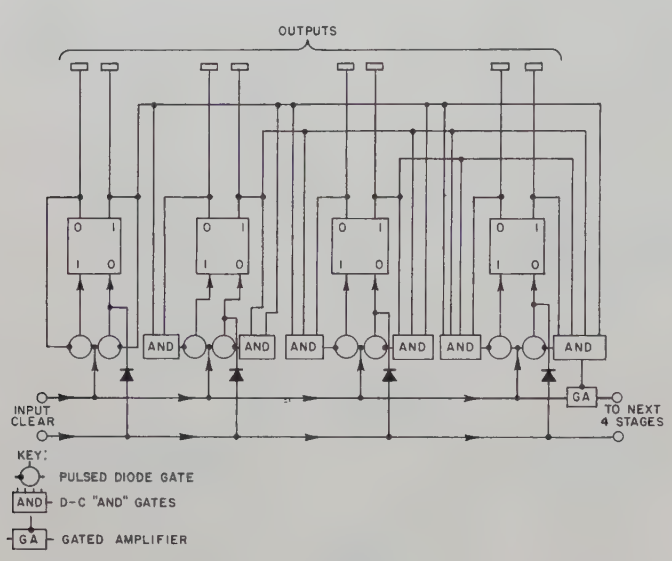

Fig. 8—Binary counter (Type 2).

Accumulator

Fig. 9 is a block diagram of a typical accumulator stage. A register of this type must have shifting and adding properties as well as several input and output gates. Input circuits cause little trouble. The number of pulsed diode gates that can be connected to the base of a flip-flop transistor is limited only by the back resistance of output diodes. "Set" and "clear" inputs, common to many stages, require the addition of a diode at the input to each stage. Although a gated pulse amplifier will supply enough pulse power to drive approximately six flip-flop inputs, a pulse amplifier can drive as many as twelve. A gated pulse amplifier followed by several pulse amplifiers will supply drive to a large register. Since the "zero" side of the flip-flop output drives only two gates, the internal emitter follower provides sufficient current. The "1" side, supplies current to five gates, requiring an additional external emitter follower. The delay circuit in Fig. 9 may be a passive delay line if its attenuation is less than 20 per cent.

Test Results

All of the switching circuits described were found to operate with supply voltage variation in excess of ±40 per cent, and at the same time deliver sufficient output to drive the appropriate load circuits. Complete interchangeability was obtained with a sample lot of about

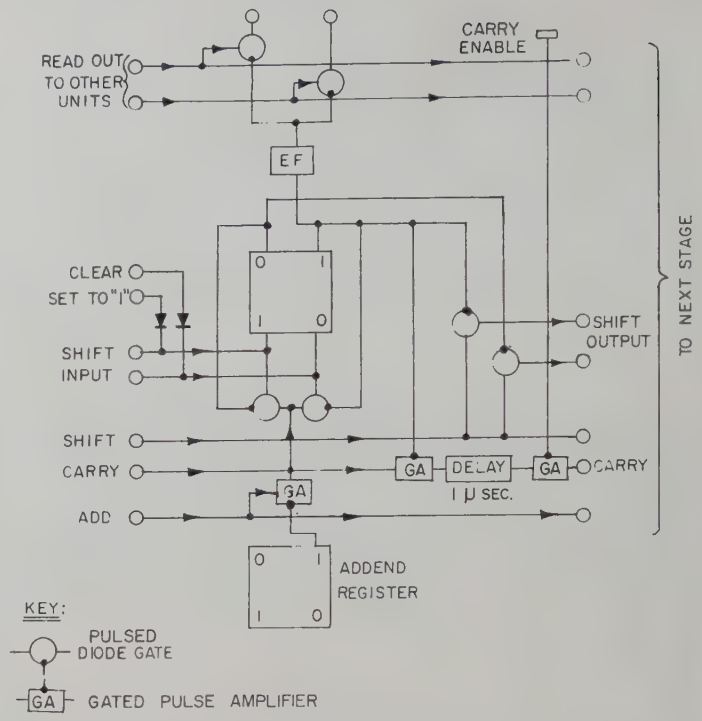

Fig. 9—Typical accumulator stage.

500 transistors which met the specifications given in Table I. Individual circuits and small subsystems were operated under varying temperature conditions. All of the circuits functioned properly between −75°C and +105°C. Life tests at +85°C are presently being conducted on a small group of transistors. After 3000 hours, all of the transistors in this group function properly. Although small variations in parameter values have been noticed, most of the transistors are still within manufacturer's specifications.[5] Thus reliable operation may be expected between −55°C and +85°C provided a suitable transistor type is selected.

Shift registers and binary counters of various "word" lengths were tested. If sufficient drive is supplied to all circuits by the liberal use of emitter followers and pulse amplifiers, registers of any length are feasible.

Conclusion

It has been shown that reliable high-speed junction transistor switching circuits can be designed. They consume very little power, operate over wide temperature ranges, and are capable of complete interchangeability. Due to ready availability and low cost of high-frequency junction transistors, complete large scale systems employing these circuits are now feasible.

Acknowledgment

The authors wish to express their appreciation to their many colleagues at Sylvania Waltham Laboratories for their invaluable aid in this work.

[5] These life test results pertain only to a transistor type with a maximum temperature rating of +85°C. Some of the available transistor types meet the electrical requirements of the circuits but have an insufficient ambient temperature rating. Therefore, selection of a suitable transistor type must include consideration of its maximum ambient temperature rating.

A Multipurpose Electronic Switch for Analog Computer Simulation and Autocorrelation Applications*

NICK D. DIAMANTIDES†

Summary—A system of four diodes in a series-parallel connection is combined with dc operational amplifiers in order to accomplish a variety of computational operations. The diode circuit is equivalent to a SPST switch survey or a voltage pulse. When inserted in series with the input of an amplifier or an analog memory, the switch makes possible waveform sampling or waveform quantizing of the input voltage. Other functions, such as the fast discharge of an integrator, are also achieved.

A very significant application of the diode switch in computer circuitry is its use in combination with a multiplier and a storer (a bank of integrators) in order to obtain autocorrelation or cross-correlation of messages after they have been translated into voltages. A commutator or a ring counter is employed to provide the switching pulse. The correlator has the advantage of generating the correlation function concurrently with the message without necessitating previous recording and repeated playback.

Introduction

THE ELECTRONIC SWITCH, which has been used in numerous applications[1] outside the computer field, is herein combined with components of a GEDA[2] electronic differential analyzer to simulate a pulse modulator and a quantizer that are important in the simulation of sampled-data control systems and the solution of difference equations. By using the switch to build an autocorrelator based on analog computer components, the usual recording and repeated-playback procedures are eliminated.

Basic Circuitry

The electronic switch consists basically of four thermionic or crystal diodes connected in series-parallel (Fig. 1). As long as the switching voltage, E, is negative

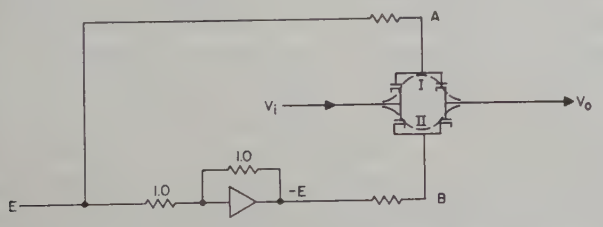

Fig. 1—Electronic-switch-circuit schematic diagram.

($E<0$), points A and B are negative and positive, respectively, and the diodes are cut off. When the switching voltage is made positive ($E>0$), points A and B become positive and negative, respectively, and all four diodes are conductive. As the result of conduction through paths I and II, a controlled voltage V_i appears at the output terminal as $V_0(=V_i)$. The condition necessary for operation of the system is $+E>|V_i|$. The impedance between V_i and V_0, if relatively appreciable, should be added to that following the output terminal. The group of four diodes corresponds to one set of single-pole, single-throw contacts; the switching voltage can be provided through any suitable control device.

Waveform Sampler

A waveform sampling circuit (Fig. 2) consisting of the electronic switch, a sampling-pulse generator, and an output amplifier can be used to provide a series of amplitude-modulated pulses (Fig. 3) whose heights repre-

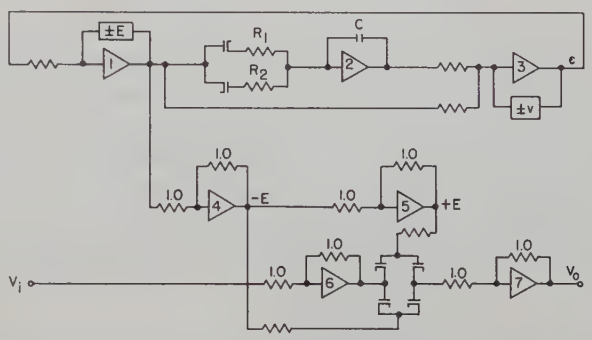

Fig. 2—Waveform sampling circuit.

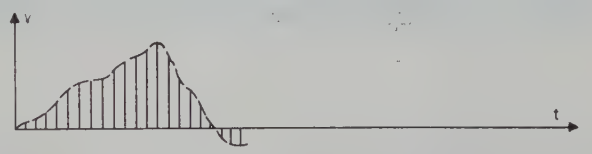

Fig. 3—Pulse-sampled signal.

sent amplitude of the sampled signal. Sampling-circuit amplifiers 1 and 3, limited to voltages of $\pm E$ and $\pm V$, respectively, have very high gains, because there is no feedback impedance across their terminals. Any negative voltage ϵ at the output of amplifier 3, however small, switches amplifier 1 to $+E$. The $+E$ voltage is applied to amplifier 3, both directly to reinforce the original voltage ϵ, and also through integrator 2 as an opposing ramp with an increase rate of

$$e = -\frac{E}{R_1C} \text{ volts/second.}$$

At the moment when $|e|>+E$, the output of amplifier 3 crosses the zero line, reversing amplifier 1 to $-E$; and the operation previously carried out through the branch R_1C is repeated through the branch R_2C. The resulting

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[1] B. Chance, V. Hughes, E. F. MacNichol, D. Sayre, and F. C. Williams, "Waveforms," Rad. Lab. Ser., McGraw-Hill Book Co., Inc., New York, N. Y., vol. 19, p. 373; 1949.

[2] Registered trademark, Goodyear Aircraft Corp., Akron, Ohio.

amplifier output switching voltage is a square wave (Fig. 4) of width t_1, separation t_2, and amplitude $\pm E$, where

$$\left.\begin{aligned} t_1 &= R_1C \text{ seconds,} \\ t_2 &= R_2C \text{ seconds.} \end{aligned}\right\} \quad (1)$$

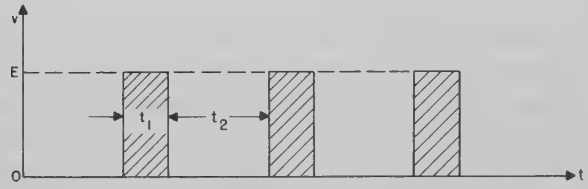

Fig. 4—Amplifier square-wave output.

The transfer function of the repetitive switch can be calculated from these values. When the input signal is time-varying $[V(t)]$ and t_1 is sufficiently small, the output is

$$\left.\begin{aligned} V_0 &= V_{(n\tau_0)} \text{ when } t = n\tau_0, \\ V_0 &= 0 \text{ when } t \neq n\tau_0, \end{aligned}\right\} \quad (2)$$

where τ_0 is the sampling period. It should be emphasized that, when the pulsing circuit is at rest, the input of amplifier 7 (Fig. 3) is effectively grounded through a resistor, because the outputs of amplifiers 4 and 5 are at zero potential. Fig. 5 shows the recorded pulse modulation of sinusoidal, triangular, and square-wave inputs. Distortion caused in the output (V_0) channel by overshoot of the recorder pen is absent when the output is observed on an oscilloscope.

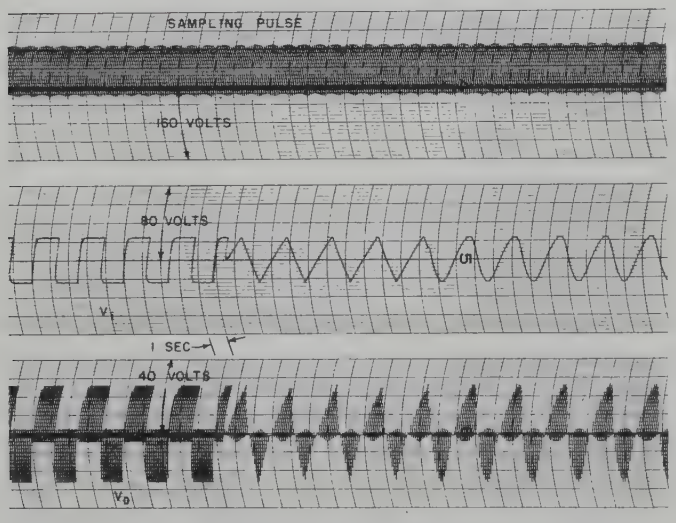

Fig. 5—Pulse modulation of sinusoidal, triangular, and square-wave inputs.

Waveform Quantizer

The waveform quantizer (Fig. 6), a modification of the sampler circuit, is distinguished by a bold feature (A, Fig. 6) that results in output equivalent to that of a "box-car" generator. The electronic switch is inserted in the forward branch of a memory loop containing only one storage element. When the switch closes, the transfer function of the closed loop is a simple time lag, $(\tau s+1)^{-1}$, with τ very small compared with sampling-pulse width. When the switch opens, the input of the end integrator is at zero potential; and the integrator output stays at the sampled value until the next sampling takes place.

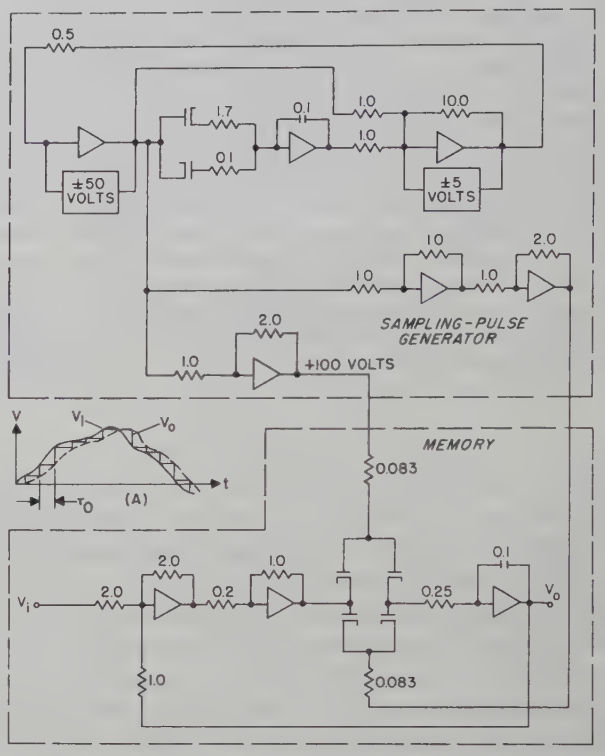

Fig. 6—Waveform quantizer.

Fig. 7 shows the results of quantization for two kinds of input sampled at the same frequency; Fig. 8 shows the quantization effect for two decaying sinusoids sampled at two different rates. It can be seen that a correlative result of the digitalization is a shifting of the sampled wave by the amount τ_0 [see Fig. 5(a)]. While this pure time-delay effect may not be satisfactory in all cases, it is believed suitable for human-dynamics studies, where the basic function of stimulus perception is accomplished in the same sample-hold manner. It was in connection with such studies that the electronic-switch circuit was first investigated. When the switch is connected in parallel with the feedback capacitor of an integrator as shown in Fig. 9, it discharges the capacitor every time the sampling pulse turns the switch on. The resulting performance when $R=1$ megohm, $C=1$ microfarad, and $V_i=100$ volts is shown in Fig. 10.

Fig. 11 shows the circuit for a gated storage unit in which positive input pulses are summed and stored. The summation of pulses resulting from the closing of manual switch S is shown in Fig. 12. A check of storage capability 10 minutes after the final voltage (e_f) was reached showed that there was no detectable loss of information of e_f. The parameter values were $R=0.1$

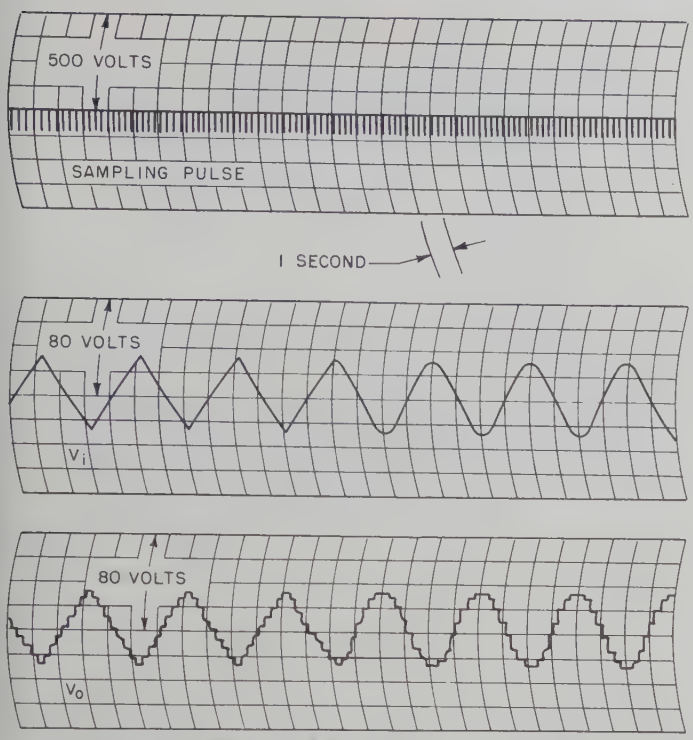

Fig. 7—Signal quantization at one sampling rate.

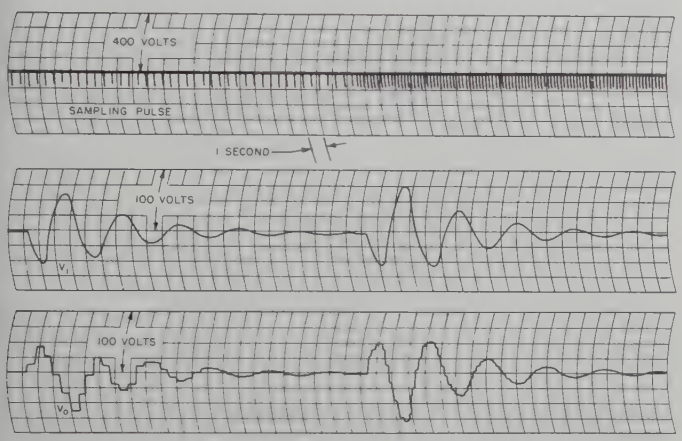

Fig. 8—Signal quantization at two different sampling rates.

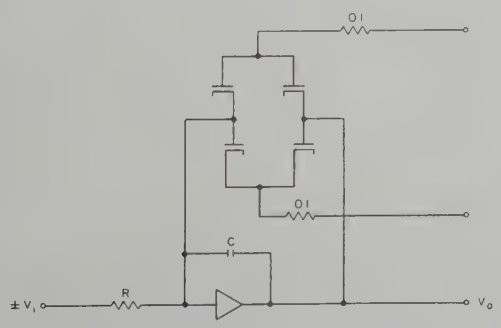

Fig. 9—Capacitor-discharge circuit.

megohm, $C=1$ microfarad, and $V_i=25$ volts. By reversing the limiter settings and the connections for the feedback diode (D) in Fig. 11, negative inputs may be stored.

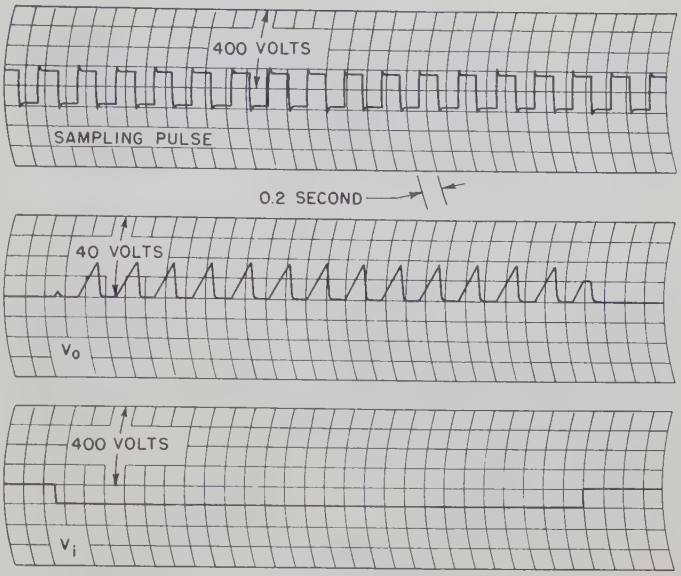

Fig. 10—Performance of capacitor discharger.

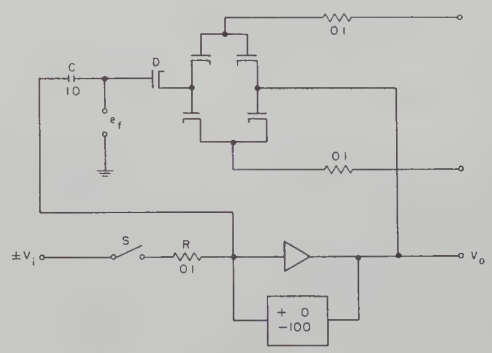

Fig. 11—Gated storage unit.

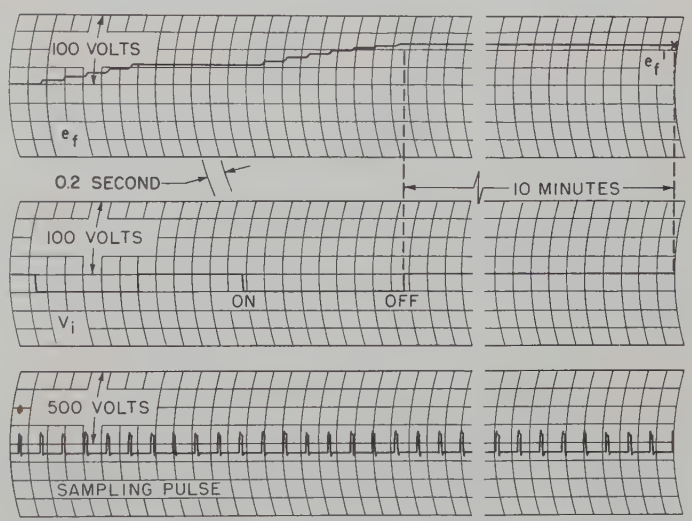

Fig. 12—Performance of gated storage unit.

The Switch as an Autocorrelator Component

Consider the analytical expression

$$A_k = \frac{1}{Nt_0} \sum_{n=0}^{N} f(nt_0) f\left(nt_0 + \frac{kt_0}{M}\right), \qquad (3)$$

where $f(t)$ is a function of time representing a message, t_0 is the quantization interval, N is the total number of samples resulting from the quantization, and $k=0, 1, 2, \cdots, M$. When N is sufficiently large, the quantity A_k becomes the autocorrelation function of $f(t)$:

$$A_k = \frac{1}{T}\int_0^T f(t)f(t+\tau_k)dt, \tag{4}$$

where $T=Nt_0$ (the message length) and $\tau_k=kt_0/M$. A_k, therefore, is an approximation of the autocorrelation function, provided that the sampling of the message fulfills the basic requirements of information theory; namely, $N=2TW$ and $(\tau_k)_{\max}>\frac{1}{2}W$, where W is the bandwidth of the message.

Suppose that the summation in (3) is written as $M+1$ separate summations.

$$\begin{aligned} A_0 &= \frac{1}{Nt_0}\sum_{n=0}^{N} f(nt_0)f\left(nt_0+\frac{0t_0}{M}\right),\\ A_k &= \frac{1}{Nt_0}\sum_{n=0}^{N} f(nt_0)f\left(nt_0+\frac{kt_0}{M}\right),\\ A_M &= \frac{1}{Nt_0}\sum_{n=0}^{N} f(nt_0)+f\left(nt_0\frac{Mt_0}{M}\right). \end{aligned} \tag{5}$$

During every sampling interval, $nt_0<t<(n+1)t_0$, the function $f(t)$ is subsampled $M+1$ times (Fig. 13), and the outcome is summed in separate storage units for each k. In this manner, the values of $A_0, A_1, \cdots, A_M$ are obtained; and the autocorrelation function of a message is produced concurrently with the message itself without requiring any special playback means.

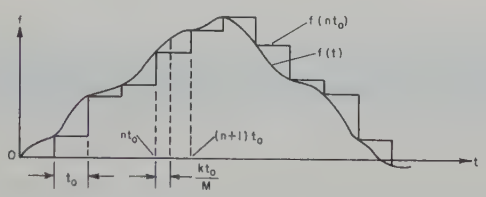

Fig. 13—Message subsampling.

Cross-correlation functions can be obtained by the same technique. The operation to be implemented will be

$$B_k = \frac{1}{Nt_0}\sum_{n=0}^{N} f(nt_0)h\left(nt_0+\frac{kt_0}{M}\right). \tag{6}$$

Fig. 14 shows a block diagram of an autocorrelator assembled on the basis of the preceding analysis. The only nonconventional component as far as the analog computer is concerned is a ring counter that connects the multiplier output to one storage unit at a time. Such a ring counter, shown schematically in Fig. 15, consists of 10 identical flip-flop stages, each an Eccles-Jordan circuit.[3] Reliable operation is assured by effecting the

[3] C. D. Tompkins and J. H. Wakelin, "High-Speed Computing Devices," McGraw-Hill Book Co., Inc., New York, N. Y., p. 23; 1950.

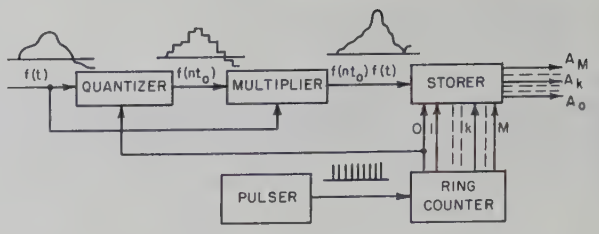

Fig. 14—Block diagram of autocorrelator using ring counter.

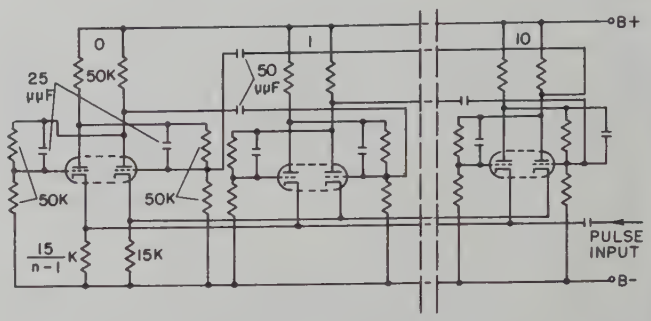

Fig. 15—Ring-counter-circuit schematic diagram.

coupling between flip-flop stages through the regular control grids with the single input terminal connected to the cathode circuits on only one side of each flip-flop. Because the pair of triodes in any stage can conduct only one at a time, the nature of the ring as a whole assures one flip-flop in the "set" state with the other nine in the reset state. Successive input signals from the pulser cause the flip-flop previously in the "set" state to resume the reset condition and simultaneously drive the succeeding flip-flop into the "set" state.

For any given pair of triodes, the two time derivatives of plate voltage obtained by means of an RC branch are pulses of opposite polarity. If the proper resistor of the diode switch is used for R in the RC branch, the switch is switched on every time the pair flips to the "set" state.

A second possibility for an autocorrelator system is shown in Fig. 16. The output of the multiplier is subsampled by means of a constant-speed commutator. Each storer integrator is connected to the multiplier for α seconds out of every t_0 seconds, where α is the time required for the brush on switch I to travel the contact arc. The brush on switch II is aligned and mechanically connected with the brush on switch I and provides the sampling pulse to the quantizer each time it wipes contact $k=0$.

The storer, shown schematically in Fig. 17, consists of 10 operational amplifiers and their associated switches, the switch of the kth amplifier being operated by the kth stage of the ring counter. The voltage representing the function to be autocorrelated, $f(t)$, is fed into both the quantizer and the multiplier. The quantizer, energized by the $k=0$ pulse of the ring counter, has its output fed to the second multiplier channel so that the product $f(nt_0)f(t)$ is obtained. Sampling of the multiplier product is then accomplished at successive instants coinciding with pulses 1, 2, $\cdots$, M of the

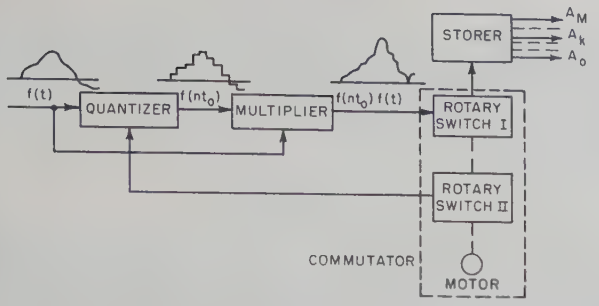

Fig. 16—Block diagram of autocorrelator using a commutator.

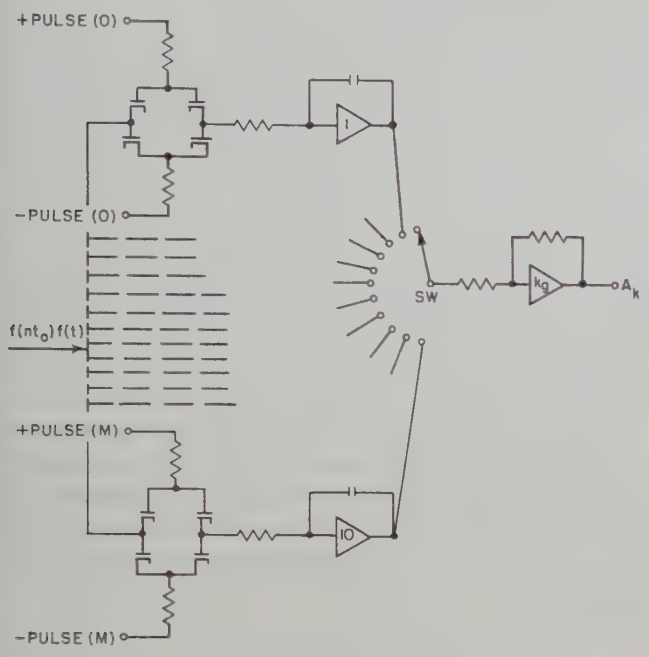

Fig. 17—Storer-circuit schematic diagram.

counter and is done in such a way that the value read by pulse number k, $f(nt_0)f(t=nt_0+kt_0/M)$, is stored in the kth amplifier. The summation continues until $n=N$; then, after a time Nt_0, the message either ceases or is switched off. Across the terminals of storer amplifier k, there is left a voltage V_k that is proportional to the value of the autocorrelogram at the point $t=kt_0/M$. The V_k voltages can be read through a read-out circuit by means of a rotary switch (SW, Fig. 17) feeding into a scale-setting amplifier. The gain k_g of the output amplifier must be calculated on the basis of the on time, t_c, of the switching pulses coming out of the ring counter; the sampling time, t_0; the time constant, RC, of the storage units; and N, the number of samplings. If, for instance, $RC=t_c$ and t_c is selected so that the multiplier output remains practically constant at v during elapse of t_c, then the output of the storage amplifier should be v at the end of t_c; and the gain must be chosen as $k_g=1/Nt_0$. It is obvious that the quantization interval t_0 must equal the maximum value of delay time τ. The autocorrelation function (8) shows the possibility that the utilized points of the term $f(nt_0)$ may not be spaced sufficiently close in some cases, but this difficulty can be resolved by using more than one multiplier-quantizer pair and additional switches. Fig. 18 shows the case where two parallel branches are used. Sampling pulse 1 of the ring counter provides the quantized value A of the term $f(nt_0)$; pulse 6 gives the quantized value B of the same term. Pulses 1 and 6 are fed into multipliers 1 and 2, actuating switches S_1 and S_2, respectively.

Two functions were tried:

$$f(t) = E \sin \omega t \tag{7}$$

and

$$P_n = \frac{(Nt)^n e^{-Nt}}{n!}. \tag{8}$$

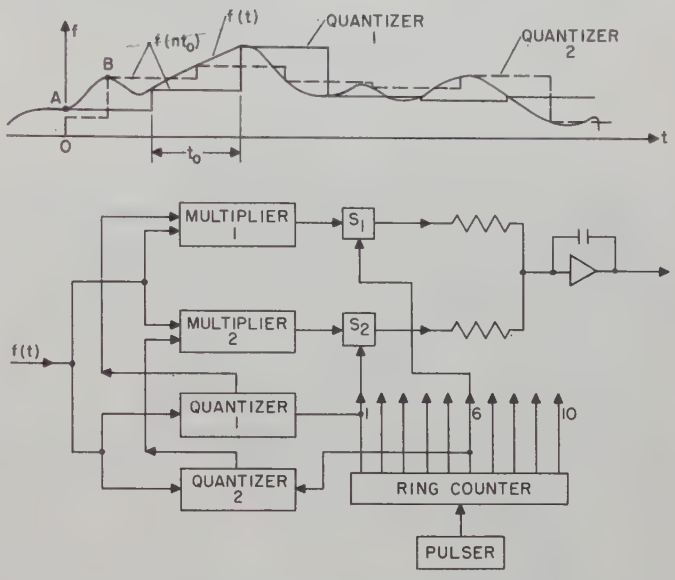

Fig. 18—Block diagram of two-branch autocorrelator.

Sinusoid

For (7), direct application of the definition of normalized autocorrelation yields

$$\begin{aligned} R(\tau) &= \frac{1}{T-\alpha}\int_{\alpha}^{T} \sin \omega t \sin(\omega t + \omega\tau)\,dt \\ &= \frac{1}{T-\alpha}\int_{\alpha}^{T} \frac{\cos \omega\tau}{2}\,dt - \frac{1}{T-\alpha}\int_{\alpha}^{T} \frac{\cos(2\omega t + \omega\tau)}{2}\,dt \\ &= \cos \omega\tau - \frac{1}{4\omega(T-\alpha)}\left[\sin(2\omega T+\omega\tau) - \sin(2\omega\alpha+\omega\tau)\right] \\ &= \cos \omega\tau - \frac{\sin \omega(T-\alpha)\cos \omega(T+\alpha+\tau)}{\omega(T-\alpha)}. \end{aligned} \tag{9}$$

For a message of sufficient length, T, the expression becomes

$$R(\tau) = \cos \omega\tau. \tag{10}$$

Curve A of Fig. 19 is the theoretical curve for $f=0.96$ cycles per second normalized to the value $R(\tau=0)$. The points along curve A denote the experimental values.

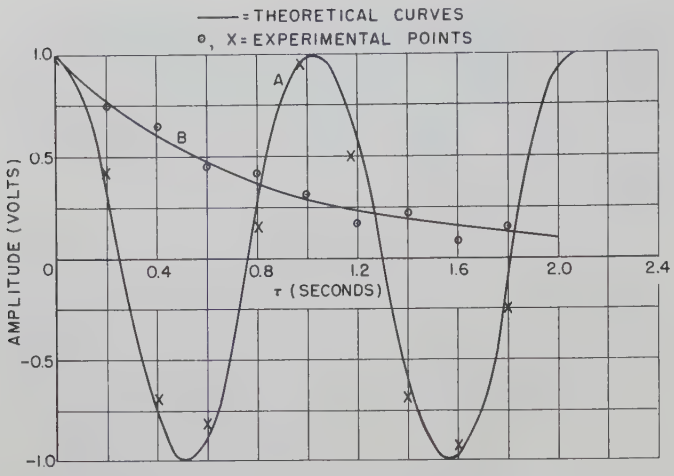

Fig. 19—Theoretical and experimental results of two auto-correlograms.

Poisson Square Wave

Eq. (8) is the Poisson probability distribution of zero crossings of a square wave having a peak-to-peak amplitude of $2E$. N is the mean number of counts per second, and the function represents the probability of n zero crossings during time t. The pulses were generated by radioactive particles triggering a Geiger tube that in turn triggered a bistable multivibrator. For the randomly spaced square wave, the correlation between signals t seconds apart is $+1E^2$ for an even number of pulses and $-1E^2$ for an odd number. The normalized correlation function[4] is therefore

$$R(\tau) = \sum_{n=0}^{\infty} (-1)^n P_n$$

$$= e^{-N\tau}\left[1 - (N\tau) + \frac{(N\tau)^2}{2!} - \frac{(N\tau)^3}{3!} + \frac{(N\tau)}{4!} - \cdots\right].$$

Because the quantity within the brackets is the Taylor-series development of $e^{-N\tau}$,

$$R(\tau) = e^{-2N\tau}. \tag{11}$$

Curve B of Fig. 19 is the theoretical curve of (16) for $N=0.625$ counts per second normalized to the value $R(\tau=0)$. The experimental points are plotted for this curve also.

Conclusion

New applications for autocorrelation and cross-correlation operations are being found in a variety of fields. Studies of noise, servoresponse to random inputs, atmospheric turbulence,[5] and ocean-wave motions require correlogram information in every step. To a certain extent, the same is true in operations research, economic studies, and the game theory. One important application of autocorrelation in communications is the wide use of correlograms in the Weiner filter theory.[6] An interesting extension of this theory attempts to extract information buried in the brain waves of an encephalogram by using autocorrelation.[7] In the case of linear time-varying systems used in process control, the correlation method is used to determine the weighting function necessary for determination of system behavior.[8]

An interesting application that demonstrates the industrial possibilities for autocorrelators is an autocorrelogram computer developed in England for analyzing the periodic components of irregularities occurring in cross sections of yarn. The periodic components can produce very undesirable patterning when fabrics are woven at certain cloth widths relative to component wave length.[9]

[4] J. W. Follin, G. F. Emch, and F. M. Walters, "Modifications and Additions to the REAC," paper delivered before Project Cyclone Symposium II, Reeves Instrument Corp., Hempstead, L.I., N. Y.; April 28–May 2, 1952. Part 2 of published papers.

[5] E. K. Webb, "Autocorrelations and Energy Spectra of Atmospheric Turbulence," Melbourne, Australia, Div. of Meteorol. Phys., Commonwealth Sci. and Ind. Res. Organization, 1955.

[6] N. Weiner, "Extrapolation, Interpolation, and Smoothing of Stationary Time Series," The Technology Press of M.I.T., Cambridge, Mass., and John Wiley and Sons, Inc., New York, N. Y.; 1950.

[7] N. Weiner, "Time and Organization" Fawly Foundation Lecture No. 2, University of Southampton, Southampton, England, p. 8, 1955.

[8] J. A. Anseltine and R. R. Favreau, "Weighting functions for time-varying feedback systems," Proc. IRE, vol. 42, pp. 1559–1564; October, 1954.

[9] J. Franklin, "Recovering of hidden signals," *Wireless World*, vol. 61, pp. 137–139; March, 1955.

Representation of Nonlinear Functions by Means of Operational Amplifiers*

ROBERT M. HOWE†

Summary—**The representation of a wide variety of nonlinear functions by means of the interconnection of unstabilized operational amplifiers is discussed. The nonlinear functions described include rectification, saturation functions, coulomb friction, dead space, and starting friction. The use of operational amplifiers alone to produce square waves and triangular waves, as well as gating operations, is also discussed. These latter circuits are combined to give a time division multiplier using only standard operational amplifiers as components. Accuracy capabilities for all of these nonlinear operations are the order of 0.01 to 1 per cent.**

Introduction

MANY OF THE nonlinearities encountered in solving differential equations do not involve multiplication of variables but instead are represented by relatively simple functions. Examples include linear terms which saturate, coulomb friction, dead-space, hysteresis, etc. In solving such problems with the electronic differential analyzer, it has been common practice to simulate the functions by combining diode circuits with operational amplifiers.[1] The purpose of this paper is to point out how the nonlinear characteristics of operational amplifiers themselves can be combined to represent a wide variety of nonlinear functions, and in many cases to represent them much more accurately than the diode-circuit counterparts.

Basic Nonlinear Characteristics of Operational Amplifiers

There are two basic nonlinear characteristics of operational amplifiers which will be described. The first of these is the saturation characteristic. Consider the operational amplifier shown in Fig. 1. With equal input and feedback resistors, the output voltage e_0 is the negative of the input voltage, except that e_0 saturates at well-defined voltages e_+ and e_- respectively. Due to the large amount of feedback, the amplifier output is extremely linear up to the saturation voltage, at which point very abrupt saturation sets in. If the feedback resistor is relatively large compared with the output impedance of the amplifier when saturated, then the saturation will be relatively flat. The output impedance when saturated will, of course, be different for positive and negative outputs and will depend on the type of output stage (conventional or cathode-follower). It should also be noted that the plate dissipation of the output tube may be exceeded during saturation in one of the two directions (positive or negative) if the amplifier has not been designed for use with a saturated output. Circuits which employ saturated amplifiers can generally exhibit accuracy from 0.1 to 1 per cent.

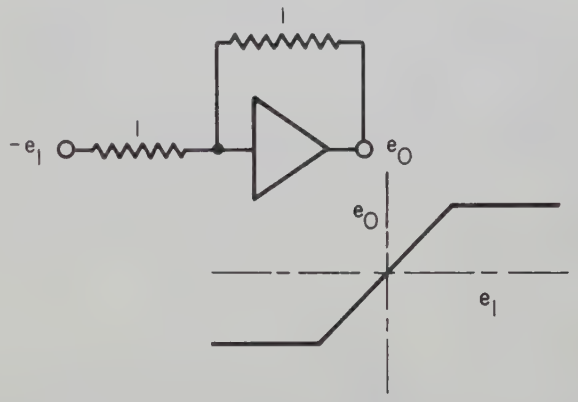

Fig. 1—Operational amplifier saturation characteristic.

The second basic nonlinearity results when the outputs of two operational amplifiers are connected in parallel, and was first described by Bradley and McCoy.[2] If the output comes from the plate of the output tube, then the amplifier which tends to have the more negative output will predominate. On the other hand, if the output comes from the cathode of the output tube (*i.e.*, the output stage is a cathode follower), then the amplifier which tends to have the more positive output predominates. This is illustrated in Fig. 2, where the upper amplifier has unity gain with the input $-e_1$, while the lower amplifier has zero gain. Whenever $e_1 > 0$, the output will be e_1; when $e_1 < 0$, the output will be zero. Thus the circuit in Fig. 2 makes an excellent half-wave rectifier. Circuits which employ amplifier outputs in parallel can exhibit accuracies as high as 0.01 per cent, with careful calibration.

It should be noted that the operational amplifiers in Figs. 1 and 2 must be operated without drift-stabilization, *i.e.*, with manual balance. Otherwise, the poor saturation recovery characteristics of the drift-stabilizer will cause large errors.

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† Dept. of Aeronautical Eng., University of Michigan, Ann Arbor, Mich.

[1] C. D. Morrill and R. V. Baum, "Diode limiters simulate mechanical phenomena," *Electronics*, vol. 25, pp. 122–126; November, 1952.

[2] F. R. Bradley and R. P. McCoy, "Voltage-limiting circuit," *Electronics*, vol. 25, pp. 121–123; May, 1955.

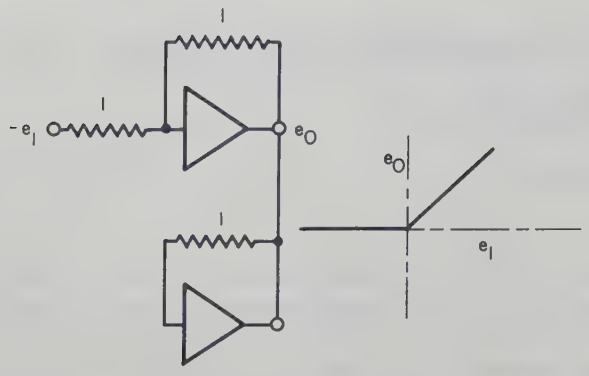

Fig. 2—Outputs of two operational amplifiers connected in parallel. The more positive predominates if cathode-follower output stages are used.

Simulation of the Saturation Function

It has already been shown in Fig. 1 that the saturation characteristics of a dc amplifier itself can be used to simulate a linear function that saturates. By selecting the proper dummy load resistor on the amplifier output, the positive and negative voltage saturation levels can often be made equal. When this is done, the circuit in Fig. 3 can be used to vary the level of saturation and still maintain unity gain.

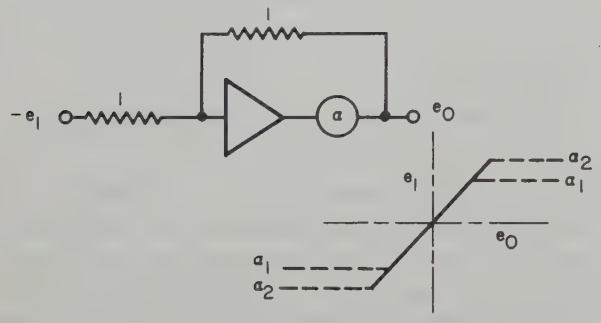

Fig. 3—Linear amplifier with variable saturation level.

A more accurate circuit for providing variable saturation levels is shown in Fig. 4. Here paralleled amplifier outputs are used, assuming that the more positive output will predominate. Although it requires four operational amplifiers, this circuit has several advantages over that of Fig. 3, including 1) separate adjustment of positive and negative saturation levels, 2) low-impedance amplifier output, and 3) better drift characteristics when the saturation levels are small compared with full scale.

Simulation of "Bang-Bang" Function, Coulomb Friction, Etc.

Often it is necessary to simulate a function which is equal to a positive constant or a negative constant, depending on the sign of the input. A "bang-bang" controller is an example, where the input is the error signal. Another example is coulomb or dry friction, where the input is velocity. The one-amplifier circuit of Fig. 3 can be used to simulate such a function if the feedback resistor is removed. Similarly, the four-amplifier circuit of Fig. 4 can also be used for this purpose if the input e_i is first fed through an amplifier with no feedback before going into amplifier 1. Finite amplifier gain and rise time limits the ideal behavior of the circuits.

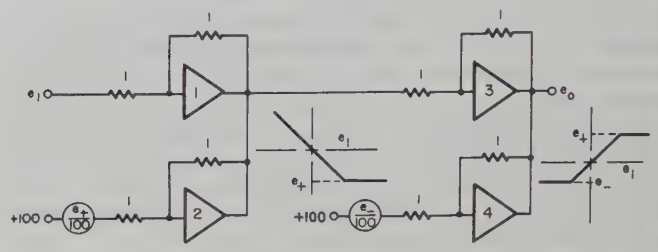

Fig. 4—High-precision circuit for saturation function.

Simulation of Additional Nonlinear Functions

Circuits for some additional nonlinear functions are shown in Figs. 5–7. The circuits for dead space are shown in Figs. 5(a) and 5(b). The circuit of Fig. 5(b)

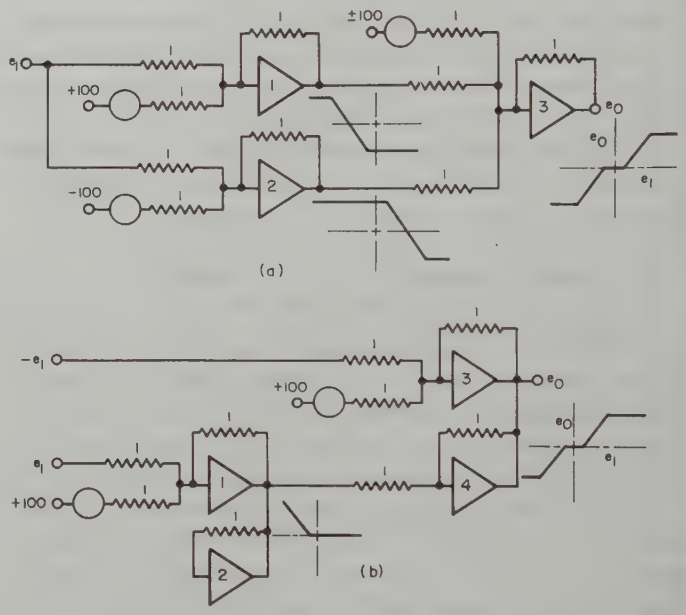

Fig. 5—Circuits for simulation of dead space. Note: By removing the feedback around amplifiers 1 and 2 in circuit (a) a "bang-bang" output with dead space is obtained.

will be more accurate but requires more amplifiers, and for most control applications the circuit in Fig. 5(a) will be completely satisfactory. In Fig. 6 is shown the circuit for simulating combined starting friction and coulomb friction, while in Fig. 7 is shown the circuit for simulating an arbitrary nonlinear function with straight-line segments. The slope of each successive section is set by the input-attenuator pot, while the ordinate of each sec-

tion is set by the bias pot. The amplifier which tends to have the most positive output will always predominate.[3] Input diodes used with a single amplifier are obviously much less complex as a function generator of this type, but if only several segments are needed and accuracy requirements are high, the circuit in Fig. 7 is quite useful.

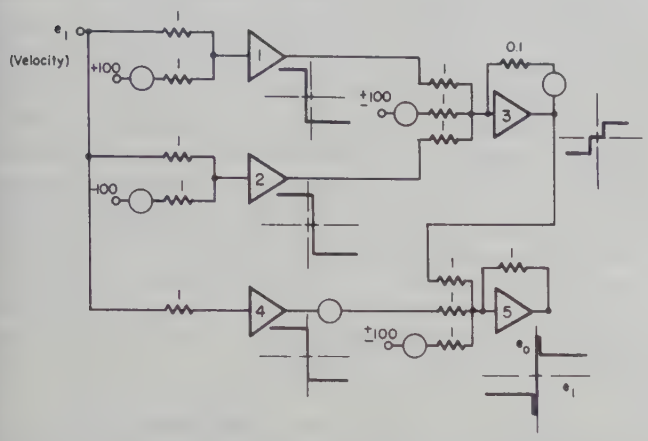

Fig. 6—Circuit for simulation *f* combined starting friction and coulomb friction.

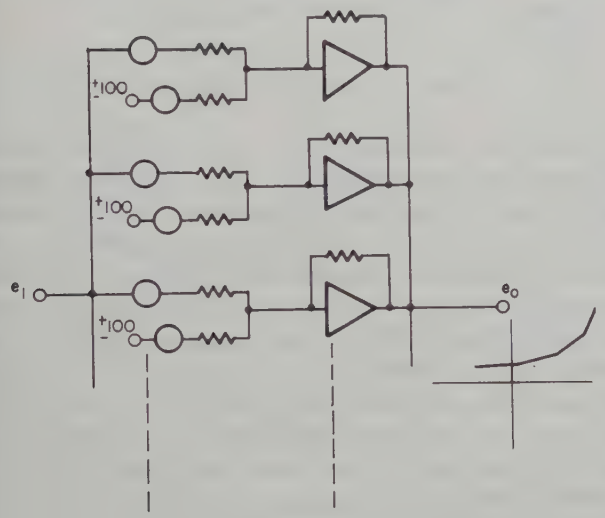

Fig. 7—Circuit for function generation.

Simulation of Hysteresis

The circuit in Fig. 8 is used to simulate hysteresis loops. It can be thought of as a first-order feedback system with either of two possible feedback paths: through amplifiers 1, 2, and 7, or through amplifiers 4, 5, and 7. Because of the presence of amplifier 3, the upper loop cannot respond to a positive error signal and integrator 7 merely holds its output voltage. That is, the upper loop can follow only increasing inputs e_i. Similarly, the lower loop can follow only decreasing inputs e_i. By means of the bias potentiometers, the dead zone is adjusted over which neither increasing nor decreasing inputs can be followed. To reduce drift effects, the RC time constant of integrator 7 should be made only small enough to allow e_0 to follow the maximum expected input velocity. The time-constant of the entire circuit is RC/α, where α is the gain of amplifier 1. The circuit of Fig. 8 gives an extremely accurate representation of the hysteresis characteristic (to within 0.01 per cent). The basic idea is based on a similar circuit employing diodes.[4]

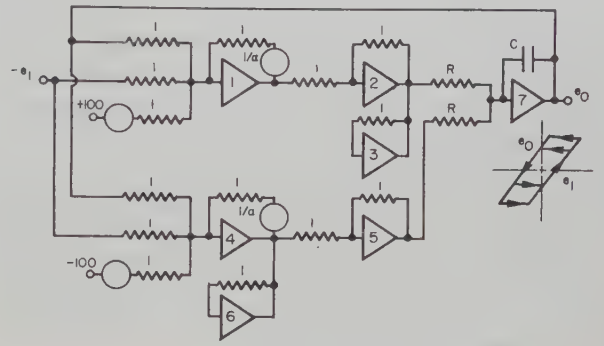

Fig. 8—Hysteresis circuit.

Gating Circuit

The availability of a good gating circuit is extremely useful in certain linear and nonlinear simulation problems. In Fig. 9 the gating circuit is again based on the fact that by connecting the outputs of two amplifiers in parallel, the more positive will predominate. By using positive or negative gating signals (normally ± 100 volts) into amplifier 2, the output will either follow amplifier 1 (*i.e.*, equal $-e_i$) or be $+100$ volts, respectively. By means of potentiometers 1 and 2 the final output e_0 of amplifier 3 is equal to e_i when the gating signal is $+100$, and is equal to zero when the gating signal is -100 volts. When $e_i = 0$, potentiometer 2 is adjusted so that e_0 does not change as the gating signal

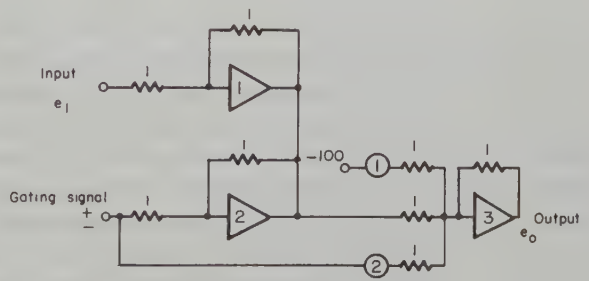

Fig. 9—Gating circuit.

[3] As shown in the figure, the circuit can be used only to simulate a function $e_0(e_i)$ whose slope increases as e_i increases. However, by adding in parallel with the outputs a second bank of amplifiers fed by $-e_i$, the case of a function with decreasing slope can also be handled.

[4] Morrill and Baum, *op. cit.*, p. 123.

is changed from + to −. Potentiometer 1 is then adjusted to bring e_0 to zero. This gating circuit is linear to better than 0.01 per cent when conducting and cuts off to within 0.01 per cent of zero when not conducting. The only obvious problem is the switchover time and accompanying transients which depend on the dc amplifier characteristics and may last from 0.1 to 5 milliseconds.

Square Wave and Triangular Wave Generator

In Fig. 10, amplifiers 1 and 2 form a bistable flip-flop circuit. Since amplifier 1 has no feedback, its output voltage will always be positively or negatively saturated. This action is intensified by the positive feedback from amplifier 2. If the output of amplifier 2 is negative, then the output of integrator 3 will increase linearly. When its output becomes something greater than +50 volts, the input grid to amplifier 1 will be driven positive and the circuit will flip to the other stable position, namely, with the output of amplifier 2 positive. This will cause the output of integrator 3 to reverse slope and decrease linearly, until its output becomes negative enough to drive the grid input to amplifier 1 negative again. The circuit then flops to its original state and the whole process is repeated periodically.

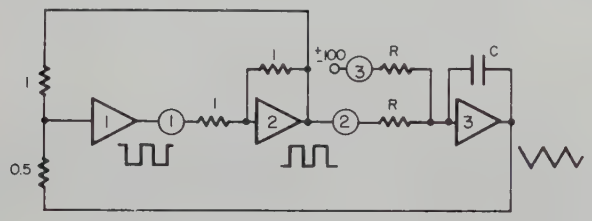

Fig. 10—Square-wave and triangular-wave generator.

The peak-to-peak amplitude of the square wave at the output of amplifier 2 is controlled by potentiometer 1, while the slope of the integrator output and hence the period is controlled by potentiometer 2. The RC time constant should be selected so that the setting on potentiometer 2 is not too low. Potentiometer 3 can be used to make the slope of one-half of the triangular wave steeper than the other half, *i.e.*, to make the half-periods of the square wave unequal. The circuit will hold amplitude and frequency to the order of 0.1 to 1 per cent. Frequencies from 0.001 to 100 cps and higher are practical for typical operational amplifiers. Note that amplifier 1 is the only one which cannot be drift stabilized in this circuit.

Time-Division Multiplier

By combining the gating circuit and triangular-wave generator described in the previous two sections, a time-division multiplier can be made. This is shown in Fig. 11, where the voltage x is summed with the triangular wave in amplifier 1. The output is a square wave with the positive-cycle duration proportional to x. This is used through amplifier 3 to gate the y voltage. The average output e_0 of amplifier 4 is proportional to the product xy. With $y=0$, potentiometer 1 is adjusted until the output e_0 does not vary for different values of x. Then potentiometer 2 is used to make $e_0=0$. Finally, potentiometer 3 is adjusted until for $x=0$ the output does not vary from zero as y is varied. If desired, a filter capacitor can be placed across amplifier 4. Potentiometer 4 controls the multiplier gain.

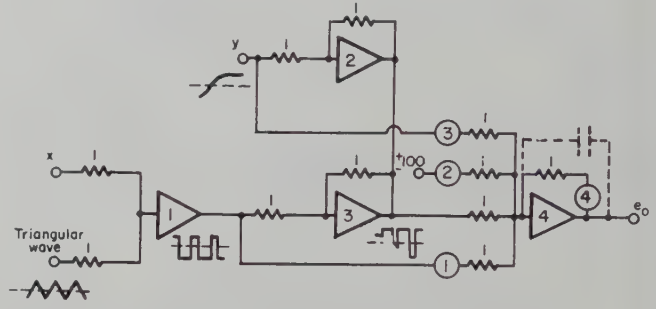

Fig. 11—Time-division multiplier.

Preliminary checks of this multiplying circuit have indicated a drift stability of 0.01 volt over several hours' time, with an over-all accuracy of approximately 0.1 per cent. These measurements were made at a repetition frequency of 50 cps which brings up the most serious limitation of this multiplying scheme, namely, its limited bandwidth. This is due to the fact that operational dc amplifiers are employed, with the result that transient switching times limit the repetition frequencies for accurate multiplication. However, the method is at least as fast as servomultipliers and apparently comparable in accuracy. The fact that only standard unstabilized operational amplifiers are employed is interesting, too. In addition to the master triangular-wave generator, four amplifiers are required for the product xy, although amplifier 4 could be used in the final circuit for summing other terms. For additional products xz, xw, etc., three amplifiers (or two if the third sums other terms) are required.

An Error Analysis of Electronic Analog Computers*

VELIO A. MARSOCCI†

Summary—Due to the physical unrealizability of electronic adding and integrating circuits with ideal characteristics, errors will be introduced in the solution of differential equations obtained by the use of electrical analog computers. Numerical errors in the solution will be introduced by fluctuations in the value of plate and of grid supply voltages, changes in the values of circuit components, and changes in the values of the vacuum tube constants. In addition, the limited frequency response of the machine components will cause the computer to solve a characteristic equation of a higher order than the original characteristic equation whose solution is desired. The error in the solution manifests itself as a shifting in the roots of the original characteristic equation as well as the production of some extra roots. The effect of this change in the root position as well as the presence of the extra roots is experienced in the curve of the solution as a function of the independent variable. In a paper on the accuracy of differential analyzers, Macnee[1] has derived an expression which gives the value of the characteristic root shift. The use of this expression is accurate only for certain types of ordinary differential equations.

In this paper a new expression for the value of the root shift is derived. The analysis preceding the new root-shift expression is developed in such a manner as to include the Macnee analysis as a special case.

Introduction

UP TO the present time, most of the literature on errors in electronic analog computers has been concerned with the tabulation of the types of errors which occur in these computers and with the development of general mathematical expressions of the error on the solution which the electronic machines give. The use of the analog machines in obtaining the solutions to various forms of differential equations has increased tremendously in recent years and it may now be advantageous to have a means of ascertaining the error in the results in terms of numerical values. Macnee[2] has considered the errors introduced by the limited response of the adder and integrating circuits, and has obtained an expression which may be used to calculate the numerical value of the characteristic root shift. The use of this expression, however, is limited to only special cases as will be shown later. Miller and Murray[3] have considered the problem from the point of view of presenting a general error analysis which evaluates the effects of errors, including the errors due to the limited frequency response of the machine components, on the machine solutions. It is the purpose of this paper to extend the work done by Macnee and arrive at a more exact expression for the characteristic root shift with a clearly defined set of conditions under which this expression remains accurate.

It has already been pointed out in the papers by Macnee and by Miller and Murray that since ideal integrating and ideal adding networks are physically unattainable, the actual system of an equation to be solved cannot be realized on the machine. This results in the machine's solving an equation of a higher order than that for which the solution is desired. The equation whose solution is desired will be referred to as the *original characteristic equation*, and the equation which the machine solves will be referred to as the *machine characteristic equation.*

In this paper on the accuracy of differential analyzers, Macnee has developed an expression

$$e_n = -\frac{1}{T_0} - T_1 s_n^2 - T_2 \frac{s_n^{m+1}}{C'(s_n)} \qquad (1)$$

for the shift in the desired roots of the original equation due to the machine solving instead, a machine system equation. In (1), e_n is the value of the root shift; T_0 is the low frequency time constant for the integrators used in the machine; and T_1 is their high-frequency time constant. T_2 is the adder time constant; s_n is the actual characteristic root of the original characteristic equation; m is the order of the original characteristic equation; and $C'(s_n)$ is the first derivative of the original characteristic equation evaluated at s_n. This expression has been found to be very limited in its application and in some cases to give inaccurate results. In this paper a new expression which is valid in general for ordinary linear differential equations with constant coefficients is developed. The new expression gives a more accurate value for the root shift than does (1). The limitations to which the accuracy of this new expression is subject are mentioned in a later part of this paper.

The machine characteristic equation for a given problem may be solved by direct means and the solution reveals, besides the presence of the extra roots, a change in the value of the roots corresponding to the original characteristic equation. The amount by which the roots are changed in value is determined by the position of these roots relative to the position of the roots of the machine characteristic equation in the complex plane. For the machine solution to be accurate, it is necessary that the roots of the characteristic equation under solution be in a region which is not appreciably influenced by the roots of the machine characteristic

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[1] A. B., Macnee, "Some limitations on the accuracy of electronic differential analyzers," PROC. IRE, vol. 40, pp. 303–308; March, 1952.

[2] *Ibid.*

[3] K. S. Miller, and F. J. Murray, "A mathematical basis for an error analysis of differential analyzers," *J. Math. Phys.*, vol. 32, p. 136; July–October, 1953.

equation. It is desirable then to have an expression for the root shift in terms of the time constants of the adding and the integrating circuits. The time constants determine the root position of the machine characteristic equation.

The Macnee Method of Estimating the Root Shift

A derivation of a characteristic equation which a machine will solve has been developed by Macnee.[4] Only the result will be considered here; the reader is referred to the Macnee paper for the actual derivation. The machine set-up shown in the Macnee paper consists of a series of integrators, with the output of each integrator being first modified by a voltage divider, which scales the integrator output to correspond to the magnitude of the coefficient in the differential equation, and then being fed back through an adder to the input of the first integrator. Macnee gives the transfer characteristic of the mth integrator in his system as

$$\frac{E_{\text{out}}}{E_{\text{in}}} = -\frac{A_{m-1}}{A_m}\,\frac{T_0}{(1+j\omega T_0)}\,\frac{1}{(1+j\omega T_1)}. \tag{2}$$

Macnee gives the over-all transfer function[5] of a differential analyzer, set up to solve the characteristic equation of

$$\sum_{n=0}^{m} A_n s^n y = F(s) \tag{3}$$

as having the form

$$1 = \frac{-\dfrac{A_{m-1}}{A_m}\,\dfrac{1}{\left[\dfrac{1}{T_0}+s\left(1+\dfrac{T_1}{T_0}\right)+s^2T_1\right]} - \cdots - \dfrac{A_0}{A_m}\,\dfrac{1}{\left[\dfrac{1}{T_0}+s\left(1+\dfrac{T_1}{T_0}\right)+s^2T_1\right]^m}}{1+sT_2}. \tag{4}$$

An inspection of (4) will show that the equation is valid only for the machine set-ups which solve characteristic equations in the following three categories:

$$A_m s^m + A_{m-1}s^{m-1} - A_{m-2}s^{m-2} + A_{m-3}s^{m-3} - A_{m-4}s^{m-4} + \cdots = 0 \tag{5}$$

$$A_m s^m - A_{m-1}s^{m-1} + A_{m-2}s^{m-2} - A_{m-3}s^{m-3} + A_{m+4}s^{m-4} - \cdots = 0 \tag{6}$$

$$A_m s^m \pm A_0 = 0. \tag{7}$$

The first two categories, (5) and (6), are comprised of equations in which the signs of the coefficients alternate beginning with, at most, the third term. For (5) no adder is needed in the machine system, and in (4), T_2 will be zero. The third category is made up of equations in which only one operator appears. This operator may be of any order. The form of the transfer function for the differential analyzer, (4), is based upon the following considerations.[6] If it is assumed that the amplifier used in the adder can be characterized in the simple fashion

$$\frac{A_0}{1+j\omega\tau} \tag{8}$$

where A_0 is the midband gain and τ the time constant of the amplifier, then the resulting expression for the adder normalized characteristic is

$$H(s) = \frac{-1}{1+sT_2} \tag{9}$$

where T_2 is the adder time constant. The approximation in the gain characteristic of the amplifier, (8), is a good one if at least one stage of the amplifier is designed so that its time constant will predominate at the high end of the band so as to determine the fall-off in the over-all amplifier gain.

If the same statements made above for the adder amplifier hold true for the integrator amplifier, then the resulting normalized transfer characteristic for the practical integrator is given as

$$H(s) = \frac{-1}{\left[s^2T_1 + s\left(1+\dfrac{T_1}{T_0}\right)+\dfrac{1}{T_0}\right]} \tag{10}$$

in (10), T_0 and T_1 are the low- and the high-frequency time constants respectively of the integrating circuit. The integrator high-frequency time constant T_1 is a function of the midband gain A_0 and of the time constant τ of the amplifier used in the integrator.

A New Method of Estimating the Root Shift

A new expression for the root shift, which applies in general to characteristic equations of (3) will now be derived. Let the characteristic equation of the original equation be written in the form

$$C(s) = \sum_{n=0}^{m} \frac{A_n}{A_m} s^n = 0. \tag{11}$$

[4] Macnee, *op. cit.*, p. 307.
[5] *Ibid.*
[6] *Ibid.*, p. 304.

For the purposes of the derivation consider as an example:

$$(A_m s^m + A_{m-1}s^{m-1} + A_{m-2}s^{m-2} + A_{m-3}s^{m-3} + A_{m-4}s^{m-4} + \cdots + A_0)y = 0. \quad (12)$$

The machine set-up which solves (12) is shown in Fig. 1. In Fig. 1, it is assumed that the output is $+y$ or that m is an even integer. In the case where m is an odd integer the final adder is not needed since the output of the last integrator is $-y$. The machine characteristic equation for Fig. 1 is

$$1 = -\frac{A_{m-1}}{A_m}\frac{1}{\left[s^2T_1 + s\left(1+\frac{T_1}{T_0}\right)+\frac{1}{T_0}\right]} - \frac{A_{m-2}}{A_m}\frac{1}{\left[s^2T_1 + s\left(1+\frac{T_1}{T_0}\right)+\frac{1}{T_0}\right]^2(1+sT_2)} - \frac{A_{m-3}}{A_m}\frac{1}{\left[s^2T_1 + s\left(1+\frac{T_1}{T_0}\right)+\frac{1}{T_0}\right]^3} - \cdots - \frac{A_0}{A_m}\frac{1}{\left[s^2T_1 + s\left(1+\frac{T_1}{T_0}\right)+\frac{1}{T_0}\right]^m(1+sT_2)}. \quad (13)$$

Multiplying through by

$$\left[s^2T_1 + s\left(1+\frac{T_1}{T_0}\right)+\frac{1}{T_0}\right]^m(1+sT_2)$$

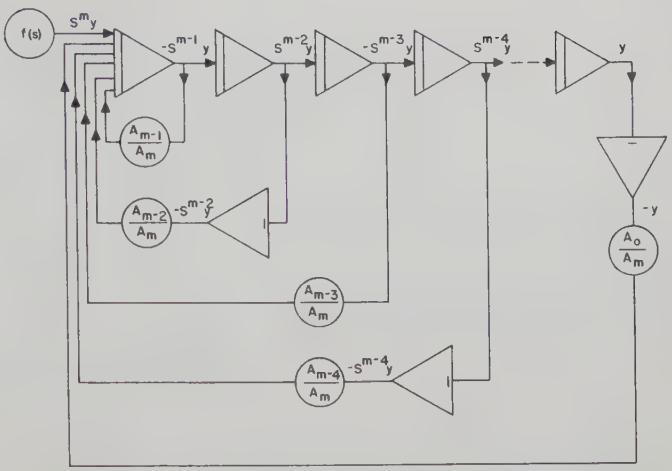

Fig. 1—Machine set-up for the solution of an mth order differential equation.

results in

$$(1+sT_2)\left[s^2T_1 + s\left(1+\frac{T_1}{T_0}\right)+\frac{1}{T_0}\right]^m = -\frac{A_{m-1}}{A_m}\left[s^2T_1 + s\left(1+\frac{T_1}{T_0}\right)+\frac{1}{T_0}\right]^{m-1}(1+sT_2) - \frac{A_{m-2}}{A_m}\left[s^2T_1 + s\left(1+\frac{T_1}{T_0}\right)+\frac{1}{T_0}\right]^{m-2} - \frac{A_{m-3}}{A_m}\left[s^2T_1 + s\left(1+\frac{T_1}{T_0}\right)+\frac{1}{T_0}\right]^{m-3}(1+sT_2) - \cdots - \frac{A_0}{A_m}. \quad (14)$$

Let

$$X(s) = \left[s^2T_1 + s\left(1+\frac{T_1}{T_0}\right)+\frac{1}{T_0}\right] \quad (15)$$

then

$$sT_2[X(s)]^m = -[X(s)]^m - \frac{A_{m-1}}{A_m}[X(s)]^{m-1}(1+sT_2) - \frac{A_{m-2}}{A_m}[X(s)]^{m-2} - \frac{A_{m-3}}{A_m}[X(s)]^{m-3}(1+sT_2) - \cdots - \frac{A_0}{A_m}. \quad (16)$$

Rearranging terms

$$sT_2[X(s)]^m = \left\{-[X(s)]^m - \frac{A_{m-1}}{A_m}[X(s)]^{m-1} - \frac{A_{m-2}}{A_m}[X(s)]^{m-2} - \cdots - \frac{A_0}{A_m}\right\} - sT_2\left\{\frac{A_{m-1}}{A_m}[X(s)]^{m-1} + \frac{A_{m-3}}{A_m}[X(s)]^{m-3}\right\} \quad (17)$$

then

$$\left\{[X(s)]^m + \frac{A_{m-1}}{A_m}[X(s)]^{m-1} + \frac{A_{m-2}}{A_m}[X(s)]^{m-2} + \cdots + \frac{A_0}{A_m}\right\} = C[X(s)] \quad (18)$$

and let

$$\left\{\frac{A_{m-1}}{A_m}[X(s)]^{m-1} + \frac{A_{m-3}}{A_m}[X(s)]^{m-3} + \cdots\right\} = \sum_{i=0}^{m} B_i[X(s)]^i \quad (19)$$

where i is a particular value of n.

By definition

$$B_i = 0 \quad (20)$$

if there is an adder characteristic associated with the ith integrator in (13), and

$$B_i = \frac{A_i}{A_m} \quad (21)$$

if there is no adder characteristic associated with the ith integrator in (13).

From (17), (18), and (19) a new function may be written

$$G(s) = C[X(s)] + sT_2\{[X(s)]^m + \sum B_i[X(s)]^i\} = 0. \quad (22)$$

Then let

$$C[X(s)] = C\left\{s^2T_1 + s\left(1 + \frac{T_1}{T_0}\right) + \frac{1}{T_0}\right\} \quad (23)$$

have roots $X(s) = s_n$, where $n = 1, 2, 3, \cdots, m$. Therefore, $C[X(s)] = 0$ for

$$T_1s^2 + s\left(1 + \frac{T_1}{T_0}\right) + \frac{1}{T_0} = s_n. \quad (24)$$

If the actual roots of (11) are designated as s_n, then the value of the shift in the roots, which may be designated as e_n, is given as

$$e_n = s_n' - s_n, \quad (25)$$

where s_n' represents the shifted root.

Using (25) and (15), let

$$X(s_n') = X(s_n + e_n) = X_n \quad (26)$$

where s_n' are the roots of the machine characteristic equation and s_n are the roots of the original characteristic equation as defined before, and e_n is the shift in the root position due to the limited response of the machine components.

From (14),

$$G(s_n') = C(X_n) + s_n'T_2[X_n^m + \sum B_iX_n^i] \quad (27)$$

where, from (26)

$$X_n = T_1s_n'^2 + s_n'\left(1 + \frac{T_1}{T_0}\right) + \frac{1}{T_0}. \quad (28)$$

From this an equation in X_n may be written as

$$H(X_n) = C(X_n) + h(X_n) \quad (29)$$

where

$$h(X_n) = s_n'T_2[(X_n)^m + \sum B_i(X_n)^i]. \quad (30)$$

Let X_{n0} be that value of X_n for which $C(X_n) = 0$, which is equivalent to saying that $X(s) = s_n$. Then expanding $h(X_n)$ around X_{n0}, and using only the first variable term of the expansion results in

$$\begin{aligned} h(X_n) &= h(X_{n0}) + h'(X_{n0})(X_n - X_{n0}) \\ &= s_nT_2[(X_{n0})^m + \sum B_i(X_{n0})^i] \\ &\quad + h'(X_{n0})(X_n - X_{n0}). \end{aligned} \quad (31)$$

Let

$$X_n - X_{n0} = \Delta X_n \quad (32)$$

then (28) may be written as

$$h(X_n) = s_nT_2[(X_{n0})^m + \sum B_i(X_{n0})^i] + h'(X_{n0})\Delta X_n. \quad (33)$$

If $C(X_n)$ is expanded around X_{n0}, and the higher order terms are also neglected, then

$$C(X_n) = C(X_{n0}) + C'(X_{n0})\Delta X_n = C'(X_{n0})\Delta X_n, \quad (34)$$

since

$$C(X_{n0}) = 0. \quad (35)$$

Eq. (29) may be written approximately as

$$\begin{aligned} H(X_n) &= C'(X_{n0})\Delta X_n + s_nT_2[(X_{n0})^m + \sum B_i(X_{n0})^i] \\ &\quad + h'(X_{n0})\Delta X_n. \end{aligned} \quad (36)$$

The value of ΔX_n which makes (29) go to zero will determine the value of s_n' for which (27) goes to zero, thus giving the desired value of e_n since s_n is already known. Then for

$$H(X_n) = 0 \quad (37)$$

$$C'(X_{n0})\Delta X_n + h'(X_{n0})\Delta X_n = -s_nT_2[(X_{n0})^m + \sum B_i(X_{n0})^i] \quad (38)$$

and solving for ΔX_n

$$\Delta X_n = \frac{-s_nT_2[(X_{n0})^m + \sum B_i(X_{n0})^i]}{C'(X_{n0}) + h'(X_{n0})}. \quad (39)$$

The evaluation of $C'(X_{n0})$ and $h'(X_{n0})$ results in[7]

$$C'(X_{n0}) = C'(s_n)\frac{1}{\left[2T_1s_n + 1 + \frac{T_1}{T_0}\right]}, \quad (40)$$

$$\begin{aligned} h'(X_{n0}) = T_2\Bigg[& mX_{n0}^{m-1}s_n + X_{n0}^m\left(\frac{1}{2T_1s_n + 1 + \frac{T_1}{T_0}}\right) \\ & + s_n\sum B_i(iX_{n0}^{i-1}) \\ & + \sum B_i(X_{n0})^i\left(\frac{1}{2T_1s_n + 1 + \frac{T_1}{T_0}}\right)\Bigg]. \end{aligned} \quad (41)$$

[7] V. A. Marsocci, "Error Analysis in Electrical Analog Computers," New York Univ. Dept. of Elec. Eng. Thesis for Master's degree, pp. 41–43; 1955.

Substituting (40) and (41) into (39)

$$\Delta X_n = -\frac{s_n T_2\left[{s_n}^m + \sum B_i {s_n}^i\right]}{T_2\left[m + \sum B_i(i{s_n}^{i-m})\right] + \left[\frac{1}{2\left[s_n + \frac{1}{2}\left(\frac{1}{T_1} + \frac{1}{T_0}\right)\right]}\right]\left[\frac{C'(s_n)}{T_2{s_n}^m} + \sum B_i {s_n}^{i-m}\right]} \tag{42}$$

and dividing each term by $T_2{s_n}^m$ and rearranging terms

$$\frac{\Delta X_n}{T_1} = -\frac{\sum B_i {s_n}^{i-m+1} + s_n}{T_1\left[m + \sum B_i(i{s_n}^{i-m})\right] + \left[\frac{1}{2\left[s_n + \frac{1}{2}\left(\frac{1}{T_1} + \frac{1}{T_0}\right)\right]}\right]\left[\frac{C'(s_n)}{T_2{s_n}^m} + 1 + \sum B_i {s_n}^{i-m}\right]}. \tag{43}$$

From (28) and (35)

$$\begin{aligned}\Delta X_n &= X_n - X_{n0} \\ &= [T_1(s_n + e_n)^2 \\ &\quad + (s_n + e_n)\left(1 + \frac{T_1}{T_0}\right) + \frac{1}{T_0}] - s_n \end{aligned} \tag{44}$$

and rearranging terms

$$\begin{aligned}&T_1 {e_n}^2 + \left[2T_1 s_n + \left(1 + \frac{T_1}{T_0}\right)\right]e_n \\ &\quad + \left[T_1 {s_n}^2 + s_n\frac{T_1}{T_0} + \frac{1}{T_0} - \Delta X_n\right] = 0. \end{aligned} \tag{45}$$

Solving (45) for e_n, the term representing the root shift, results in

$$e_n = -\frac{1}{2T_1}\left[2T_1 s_n + \left(1 + \frac{T_1}{T_0}\right)\right] \pm \frac{1}{2T_1}\sqrt{\left[2T_1 s_n + 1 + \frac{T_1}{T_0}\right]^2 - 4T_1\left[T_1 {s_n}^2 + s_n\frac{T_1}{T_0} + \frac{1}{T_0} - \Delta X_n\right]}. \tag{46}$$

It can be shown that the shift, e_n, is given by the expression containing the positive radical term. Eq. (46) may be written in the form

$$\begin{aligned}e_n &= -\frac{1}{2T_1}\left[2T_1 s_n + \left(1 + \frac{T_1}{T_0}\right)\right][1 - \sqrt{1 - \delta}] \\ &= -\left[s_n + \frac{1}{2}\left(\frac{1}{T_1} + \frac{1}{T_0}\right)\right][1 - \sqrt{1 - \delta}] \end{aligned} \tag{47}$$

where

$$\delta = \frac{4T_1\left[T_1 {s_n}^2 + s_n\frac{T_1}{T_0} + \frac{1}{T_0} - \Delta X_n\right]}{\left[2T_1 s_n + 1 + \frac{T_1}{T_0}\right]^2}. \tag{48}$$

In Table I a tabulation of results is shown, in which the root shifts, calculated by the use of (47), for the machine solutions of the equation for simple harmonic motion

$$\frac{d^2y}{dt^2} + \omega_0^2 y = 0 \tag{49}$$

and of the hyperbolic equation

$$\frac{d^2y}{dt^2} - \omega_0^2 y = 0 \tag{50}$$

are compared with the exact root shifts. The table also includes the result of applying (47) to a second order differential equation which has as a characteristic equation

$$\frac{d^2y}{dt^2} + 2\omega_0\frac{dy}{dt} + 2\omega_0^2 y = 0. \tag{51}$$

The values for T_0, T_1, and T_2 used for purposes of calculation are given in the appendix.

The root shift as calculated by the use of (1) is arrived at by approximations[8] based on the statements

$$\frac{1}{T_0} \ll s_n \ll \frac{1}{T_1}, \frac{1}{T_2}. \tag{52}$$

Therefore, the accuracy of (1), in giving the root shift, is limited by the extent that the values of T_0, T_1, T_2, and s_n for any particular problem meet the criteria stated by (52).

A new expression, (47), has been derived which gives the root shift explicitly in terms of T_0, T_1, and T_2, the integrator and the adder time constants, and s_n, the actual root position of the original characteristic equation. An approximation is involved in the derivation of (47) since the higher order terms of a Taylor's series expansion (31), are neglected. From the tabulation of results in Table I, which shows a comparison of the root shift calculated by (47), with the exact root shift, it is clear that the new equation gives a good estimate of the root shift.

[8] Macnee, *op. cit.*, p. 306.

TABLE I

COMPARISON OF THE ROOT SHIFT CALCULATED BY (47) WITH THE EXACT ROOT SHIFT

	Exact Root Shift	Root Shift Calculated by (47)
Equation for Simple Harmonic Motion, (49). (Original roots at $s=\pm j10$).	$-0.195\pm j0.050$	$-0.1935\pm j0.054$
Hyperbolic Equation, (50). (Original roots at $s=\pm 10$).	-1.65	-1.64
Second Order Equation, (51). (Original roots at $s=-10\pm j10$).	$-0.238\pm j1.680$	$-0.271\pm j1.725$

The results using the new expression, (47), are not only more accurate numerically than the results obtained by the use of (1), but the imaginary part of the root shift which is lost through the use of (1), in the case of the simple harmonic motion equation, is included in the result given by (47). The use of (47) is valid for estimating the root shift for characteristic equations of any ordinary linear differential equation with constant coefficients when these equations are solved on an electronic analog computing machine.

Appendix

Calculation for Exact Root Shift

A specific example may be used to show the method of calculating the exact position of the roots of the machine characteristic equation. Consider purely for purposes of calculation, that T_0, the integrator low-frequency time constant, is equal to 1 second, and that T_1 and T_2, the integrator high-frequency time constant and the adder time constant, respectively, are equal to 5.4×10^{-3} second. In integrators the value of T_0 will be very much larger than one second. The value of $T_0=1$ second was chosen here for ease in calculating the results shown in Table I. Since the adder in most types of equipment uses the same amplifier as the integrator, its time constant will be assumed as equal to the integrator high-frequency time constant.

Consider the second order differential equation which has as a characteristic equation

$$\frac{d^2y}{dt^2}+2\omega_0\frac{dy}{dt}+2\omega_0^2y=0. \tag{53}$$

The roots of the characteristic equation are located on the complex plane at

$$s_n=-\omega_0\pm j\omega_0. \tag{54}$$

Assume $\omega_0=10$, for purposes of calculation so that

$$\frac{0.1}{T_1},\ \frac{0.1}{T_2}>s_n>\frac{10}{T_2}. \tag{55}$$

The machine set-up for the solution of (53) is shown in Fig. 2. Considering the characteristics for the practical integrator and the practical adder given by (9) and (10),

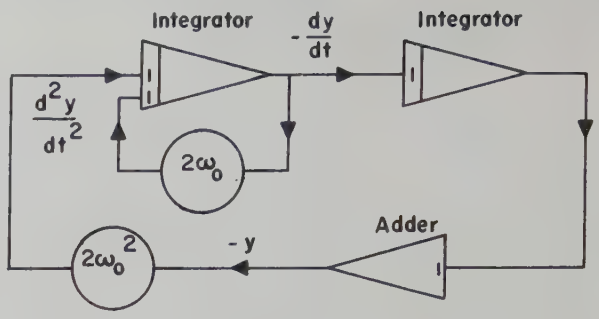

Fig. 2—Machine set-up for the solution of a second order differential equation.

the machine solves its own system equation which, when transformed, is given as

$$y=\frac{-2\omega_0^2T_0^2y}{(1+sT_0)^2(1+sT_1)^2(1+sT_2)}-\frac{2\omega_0T_0y}{(1+sT_0)(1+sT_1)}. \tag{56}$$

Multiplying out, and substituting the value $\omega_0=10$, then for $T_0=1$ second and $T_1=T_2=5.4\times10^{-3}$ second, (56) results in

$$s^5+s^4(557.56)+s^3(107.69\times10^3)+s^2(7.9258\times10^6)+s(141.19\times10^6)+(1403.5\times10^6)=0. \tag{57}$$

The roots of this fifth order equation are

$$s_1,\ s_2=-10.238\pm j11.68, \tag{58}$$

$$s_3,\ s_4=-171.05\pm j26.00, \tag{59}$$

$$s_5=-195. \tag{60}$$

The first set of roots (58), represents the shifted roots corresponding to the roots of the characteristic equation of (53). Comparing the result with the actual roots of the original equation (53), which shall be designated s_n, it can be seen that the shift in the roots may be given as

$$e_n=s_n'-s_n \tag{61}$$

where s_n' represents the shifted root and e_n has the value

$$e_n=-0.238\pm j1.68. \tag{62}$$

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Pulse Generator and High-Speed Memory Circuit*

Z. BAY† AND N. T. GRISAMORE‡

Summary—**Circuits for the recycling of pulses by means of a driving tube and an electromagnetic delay line have been developed. The necessary characteristic for the driving tube is shown and the effects of the delay line on the amplitude and width of pulses with respect to recycling operation are explained. Two modes of operation of these circuits are possible. One mode of operation allows any number of pulses in a recycling period, the number being limited only by the time space on the delay line. The other mode restricts the number of pulses in a recycling period to a particular value.**

Experimental circuits are shown which have been used as generators of pulses as short as 5 millimicroseconds at frequencies as high as 50 mc. Other circuits are shown which can be used as memory circuits for the storage of a number of these short pulses.

Introduction

THE RECYCLING of electrical pulses by means of a feedback system consisting of a coaxial cable and a driving circuit (Fig. 1) can be used either

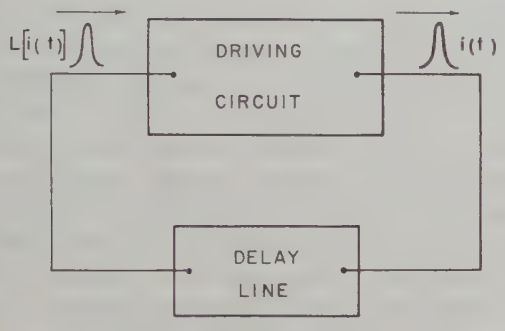

Fig. 1—Block diagram of recycling circuit.

as a memory circuit[1] or as a generator of short pulses at a high prf (pulse repetition frequency).[2] This paper describes the work done on a recycling system using amplifier tubes having one or more stages of secondary emission amplification. This system produces pulses as short as 5 mμsec at a prf up to 50 mc and will store as many as 20 pulses in a μsec length of cable. This work, begun in 1950, was intended to develop a high-speed memory for use in computing machines but the circuit can also be used to test devices responding to short pulses.

It was desired that the recycling system should be of a simple form (Fig. 1) and that it should produce output pulses of reasonably high power ($\sim$1 watt) having a width in the mμsec range. The circuits in this paper, consisting of only a driving tube and a time delay network, will produce output pulses of the above specifications.

Since the feedback network broadens and attenuates the recycled pulses it is obvious that the driving tube must perform a nonlinear operation which will resharpen and amplify the pulses. Therefore, the action of the circuit in a stable recycling operation can be represented by the relation,

$$i(t + T) = N\{L[i(t)]\},$$

where L and N are linear and nonlinear operators respectively, representing the action of the linear and nonlinear parts of the circuit, and $i(t)$ is the current pulse delivered to the *input* of the delay network by the driving tube. The function $i(t+T)$ represents the current pulse at this *input* point after a period, T, which is the sum of all of the delays in the circuit.

A mathematical treatment of this operation using a power law, nonlinear operator, and a Gaussian pulse shape has already been presented.[2] The solution was given for a circuit using an automatic volume control based on constant pulse repetition frequency. Since this solution will not apply for the recycling of an indefinite number of pulses (memory device) in a period T and since an exact treatment of the relation between $i(t)$ and $i(t+T)$ requires an accurate knowledge of N and L, a graphical representation of the current relations was used to determine the tube characteristics necessary for the recycling operation. Assuming that the $i(t)$ function is of the form shown in Fig. 2(a), it is reasonable to expect the input to the driving tube, $L[i(t)]$, to be of the form shown in Fig. 2(b). This is the general voltage response of a linear network to a current pulse of the shape of $i(t)$. The operator N can be represented by the transfer characteristic shown in Fig. 2(c). This may be taken as the transfer characteristic of the driving tube provided that transit time spread in the tube is much shorter than times associated with the pulse (rise time, decay time, period of the fundamental frequency, etc.). It can be seen that N should shorten the pulse so as to overcome the lengthening produced by L. At the same time, the slope of N (the transconductance) at the point M should be less than the slope of a line drawn through C and M. Stable recycling operation will result from this condition since pulses slightly smaller than the one shown will be amplified with loop gain >1 around their maximum and, conversely, pulses slightly larger will be amplified

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[1] Natl. Bur. of Standards Rep. No. 1245, "Computing Machine Components Program," Corona Labs.; July/September, 1953.

[2] C. C. Cutler, "The regenerative pulse generator," PROC. IRE, vol. 43, pp. 140–148; February, 1955.

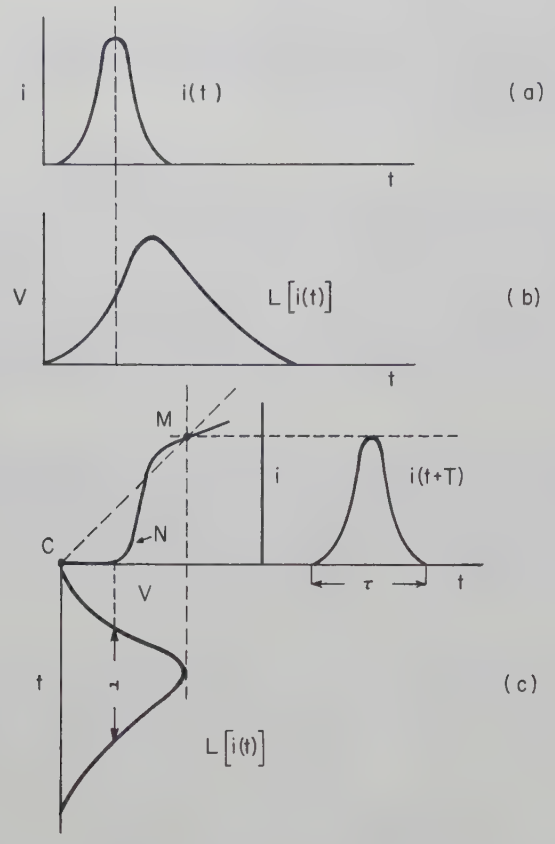

Fig. 2—(a) Current pulse output of driving circuit as a function of time. (b) Voltage pulse as a function of time resulting from a linear operation on the current pulse, $i(t)$. (Linear operation means that the superposition principle can be applied.) (c) Operation on the voltage pulse, $L[i(t)]$, by the tube transfer characteristic, N, to produce an output current pulse of the same size and shape as in (a).

with a loop gain <1. This is necessary when the bias, C, is not a function of the pulse frequency.

Experimental Circuits

Driving Tubes

The characteristic shown in Fig. 2 can obviously be obtained from a conventional voltage amplifier but two stages of amplification will be needed if the input point is the control grid because of the phase reversal obtained with just one tube.[3] The disadvantage of a two-tube driving circuit is that one of the tubes must be operated with a steady current equal to the peak-pulsed current in the delay line and must have a characteristic as sharp as that of the tube driving the delay line.

A conventional grounded-grid, single-tube, driving circuit cannot be used since the power gain around the loop will be less than one. The external losses can be compensated, however, if there is a current amplifying section in the tube. There are a number of tubes available at present which have secondary-emission current multiplying electrodes between the control section and the anode. The commercial types (*e.g.*, the Philips EFP-60, the National Union 5857, and the E.M.I. Z319/6351) have one stage of multiplication. The authors have constructed a number of tubes having seven stages of current multiplication. The reason for using a large number of stages was to be able to operate the control section in the region of low currents (μamp) thereby obtaining a transfer characteristic which was essentially logarithmic (very steep) until space-charge effects limited the current.

The authors have used both the Philips tube and the seven-stage tube as driving tubes in recycling circuits. The pulsed power output obtained from each tube was about the same (*e.g.*, 100 ma into a 72-ohm cable). The minimum pulse widths were about the same since the input and output capacitances of the two tubes are of the same magnitude. However, because of the sharper characteristic curve of the seven-stage tube more attenuation can be tolerated so that longer delay lines can be used with this tube. The allowable power dissipation is also greater for the seven-stage tube so that a greater duty cycle is permissible.

Recycling Circuit

The circuit consists of a delay line, a driving tube, and an input and output network for the driving tube. Usually the low impedance cables ($Z \approx 50$ ohms) have less high-frequency attenuation which is offset in this application by the resulting lower pulse voltage. We have used cables of various lengths ranging in impedance from 50 to 125 ohms. The lower impedance cable usually resulted in sharper pulses, whereas longer delay times and greater pulse widths were obtained with the higher impedance cables. These results were, of course, also dependent on the type of driving tube.

The output of the driving tube, usually the plate, can be either ac or dc connected to the delay line. Of necessity, the output point must operate at a dc voltage different than that of the input. There must, therefore, be capacitive coupling between the input and output unless batteries, vr-tubes, dropping resistors, or other suitable dc devices are used. This capacitive coupling can be located at either end of the delay line depending on whether the line is dc coupled to the input or output. During a pulse period the voltage across this coupling capacitor will change. If the capacitor does not recharge completely in the period between pulses then, after a few cycles, a typical multivibrator action will occur whose frequency will be governed by the time constant given by the coupling capacitor and its shunting resistance. This resistance consists of that represented by the tube and the external circuit. There are two ways of overcoming this effect; either the capacitance should be so small that the time constant will be shorter than the time-length of the delay line or diodes can be inserted in the circuit so that the capacitor is recharged after a period of the order of the pulse length; both systems have been used.

[3] If one had a transformer that would operate at high frequencies without considerable loss then a one-tube circuit could be designed. Such transformers at present are not available commercially, although laboratory types have been constructed.

The input circuit can be adjusted such that its impedance is almost equal to the characteristic impedance of the delay line. This, of course, is complicated by the nonlinear impedance represented by the driving tube or any diodes in the circuit. (The effect of a nonlinear impedance is not included in N.) A fairly good match can be achieved by adding resistance in parallel with the input and observing the reflections that occur on the cable. Matching in this manner has shown the operation of the circuit to be relatively insensitive to cable matching.

Most of the results presented here were obtained with the EFP-60 tube although the seven-stage tube was also used considerably. The circuits are shown in Fig. 3 in the order in which they were developed. In Fig. 3(a) and 3(b) the resistors, R_p, are used only to provide a dc connection for the plate and should be much larger than the cable impedance so as not to attenuate the output signal. On the other hand, the capacitors, C, must be small since they are recharged, after a pulse, through R_p which is large. This, of course, means a loss in input since C is connected to a low impedance point and an appreciable portion of the output will appear across C. This situation will not exist in the circuits of Fig. 3(c), 3(d), and 3(e). Here, the capacitors can be large since they will be recharged rapidly through the diodes and the low input impedances. The diodes also serve to damp out oscillations that would occur in the output.

The plate and cathode resistors, R_p and R_k, can be varied from 220 to 1200 ohms without greatly affecting the recycling operation. The lower values produce shorter pulses but, of course, require higher current output from the tube. The coupling capacitors, C, in Fig. 3(a) and 3(b), ranged in size from 10 to 1000 $\mu\mu$f for the seven-stage tube and from 10 to 200 $\mu\mu$f for the EFP-60 tube, depending on the length of delay line, shorter lines requiring the use of smaller capacitors. Coupling capacitors as large as 0.1 μf were used in the circuits of Fig. 3(c), 3(d), and 3(e). The size of the chokes, L, was varied from 0.47 to 10 μh. Chokes outside of this range were not investigated. As previously pointed out, the duration of the pulses is determined principally by the characteristic of the driving tube. However, the value of the choke also has some effect on the pulse duration.

At first glance it would seem that the circuits of Fig. 3(a) and 3(c) would be superior with respect to the effect of parasitic capacitance to those of Fig. 3(b), 3(d), and 3(e). However, the cable impedance and the inductance, L, or the resistance, R_p, are a parallel load on the output in Fig. 3(a) and 3(c), whereas, in Fig. 3(b), 3(d), and 3(e), the only load on the output is the cable impedance. The circuit of Fig. 3(e) gave narrower pulses than the others for delay lines longer than 0.1 μsec. For delay times shorter than this there is only a slight difference in the performance of the circuits.

The delay cable used for most of the work was RG-62/U (93 ohms). This represents a compromise between attenuation and impedance. The power dissipation of the tubes limited the minimum time length of the delay lines to about 20 mμsec. Delay lines as long as 350 meters (1.75 μsec for RG-59/U) were used with the

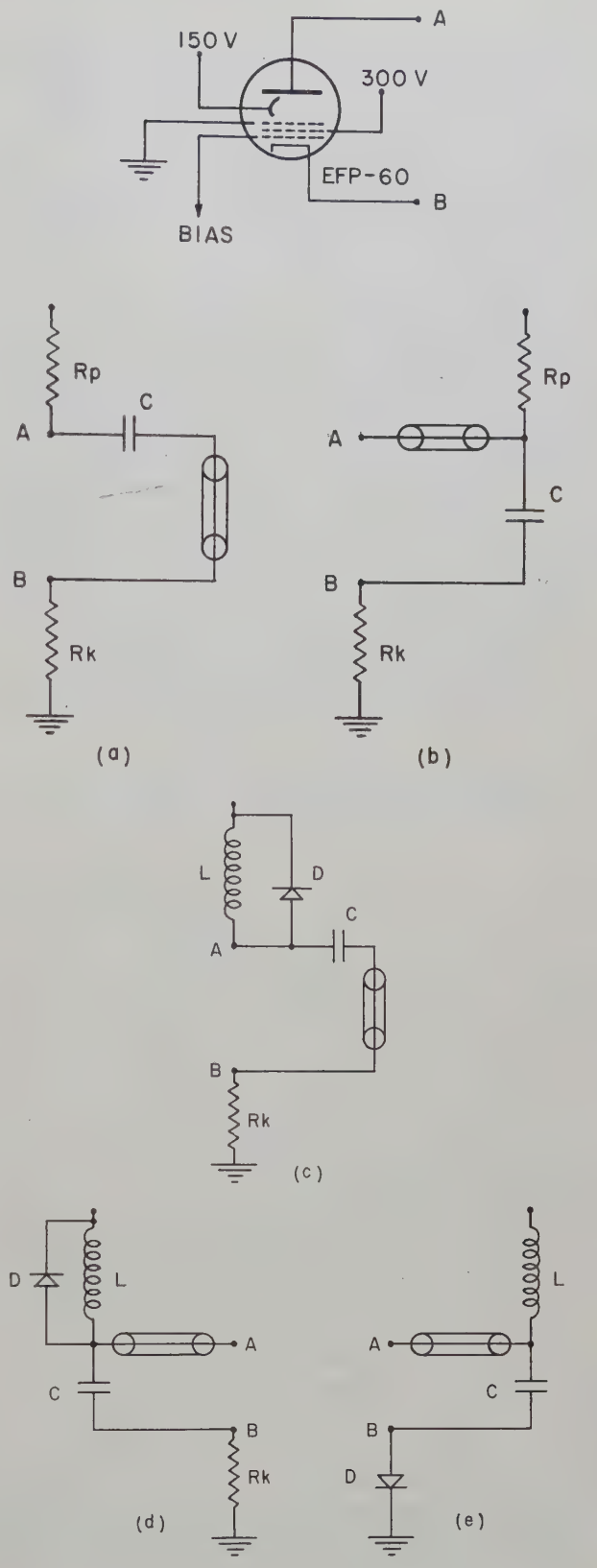

Fig. 3—Types of recycling networks which have been used in pulse generator circuits.

seven-stage tube while 125 meters (0.5 μsec for RG-62/U) was the limit when the EFP-60 tube was used. These are not really limitations for the use of this device as will be shown later. A lumped constant delay line with a characteristic impedance of 50 ohms, a delay of 0.1 μsec, and a bandwidth of 127 mc was also used. Because of the limited bandwidth, the pulses were of longer duration than those obtained with RG-62/U coaxial cable.

Two different modes of operation are possible with the circuits shown in Fig. 3. In one case the tube can be self-biased so that the bias voltage is determined by the duty cycle of the pulses. Such a biasing arrangement is shown in Fig. 4(a). For a particular setting of the potentiometer recycling will occur only within a limited range of duty cycle. It should be noted that stable operation for this mode is not established until after a time greater than CR_B and also that the length of the delay line determines the duty cycle both by its time length and its effect on the width of a pulse.

The second mode of operation results from having a bias which is not affected by the recycling. This type is shown in Fig. 4(b). Of course there is always some dc

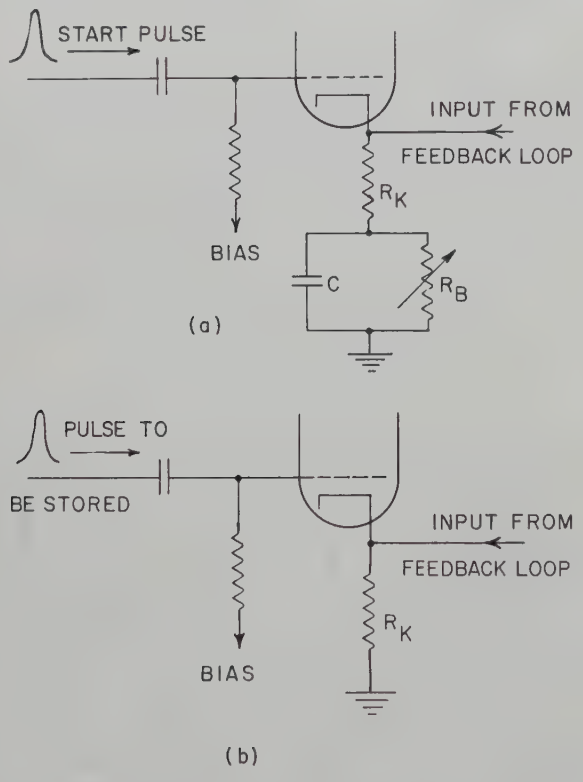

Fig. 4—Biasing arrangements for the two modes of operation. (a) Biasing for constant frequency recycling pulse generator. (b) Biasing for memory circuit.

voltage generated across R_k in both circuits but its magnitude is very small compared to the input signal and the bias amplitudes. This is evidenced by the fact that for this biasing the duty cycle has very little or no influence on the recycling operation. Actually, circuits with this type of biasing have been operated with duty cycles ranging from less than 10 per cent to greater than 50 per cent.

Application of Experimental Circuits

A recycling circuit of the general type shown in Fig. 1 can be used for two different purposes. When self-biasing is employed, a pulse generator having a stable prf results if the bias is adjusted so that only one pulse recycles through the circuit. A typical circuit of this type is shown in Fig. 5. The recycled pulses are about

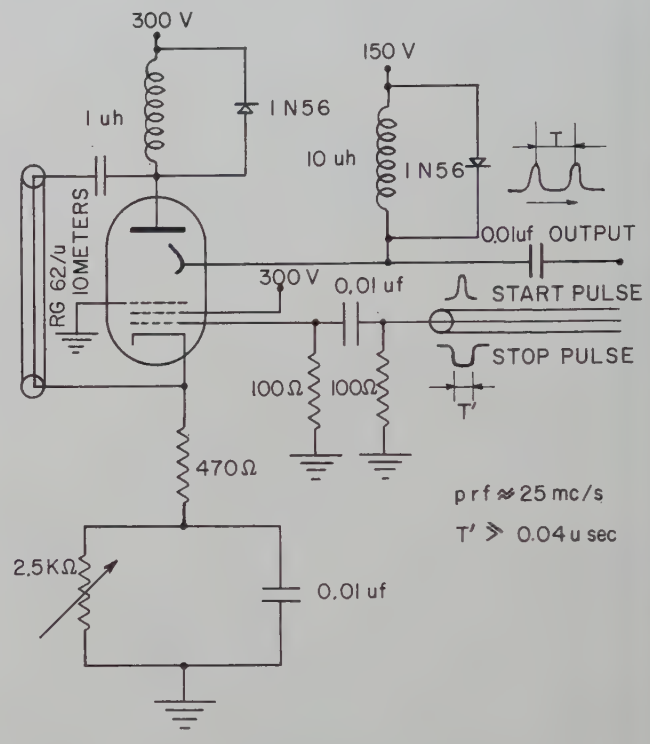

Fig. 5—Complete circuit for a recycling pulse generator of frequency ≈25 mc.

10 mμsec wide and have an amplitude of about 8 volts at the anode. With this circuit it is possible to obtain output pulses from the dynode of amplitude greater than 10 volts with a load of 10 μh in parallel with a 1N56 diode. Since the output capacitance of the dynode is about 50 per cent greater than that of the anode, the rise of the dynode pulse will not be as fast as that of the anode pulse. Pulses as short as 10 mμsec can be obtained from the dynode but the amplitude will be only 3 volts.

When an external bias is used the circuit can be employed as a memory device. From zero to n pulses can be inserted and stored in the system in the same manner as any other delay-line storage system (*e.g.*, a mercury delay-line system). A typical circuit of this type is shown in Fig. 6. This particular circuit can store six pulses in one period (0.5 μsec). A similar circuit using

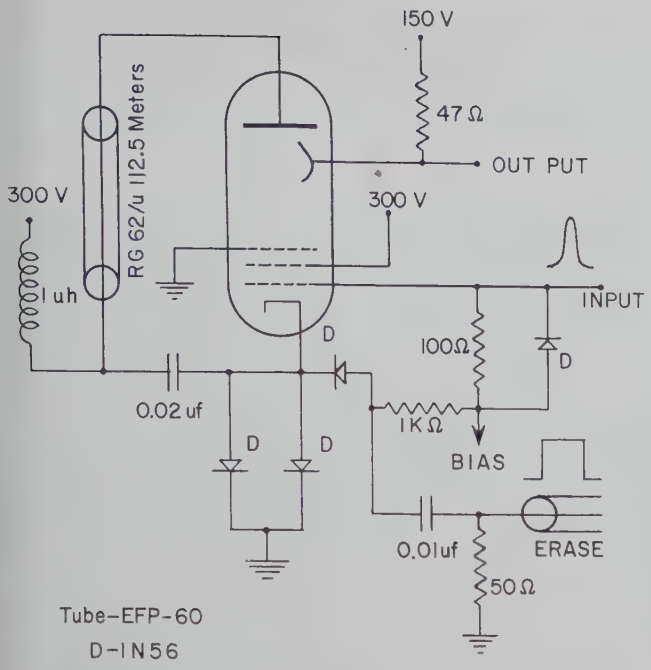

Fig. 6—Complete circuit for a memory device. Six pulses can be stored in the recycling period of approximately 0.5 μsec.

the seven-stage tube could store twenty pulses in a period of one μsec. The shortest pulses (5 mμsec) were obtained with the circuit shown in Fig. 7. There was

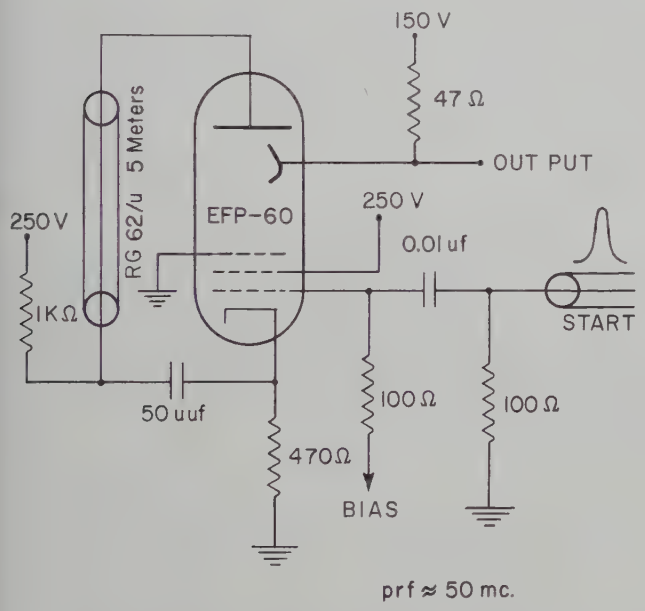

Fig. 7—Recycling circuit used to produce output pulses of about 5-mμsec duration at a rate of 50 mc.

some ringing evident when these pulses were observed directly on the deflection plates of a 517 Tektronix Oscilloscope. Presumably the ringing could have been somewhat damped if a diode had been used in place of the cathode resistor.

If one desires a short pulse, *e.g.*, 5 mμsec, recycled with a lower prf or if it is desired to have a memory circuit with a higher pulse-time density (pulses/unit time) then it is necessary to use more than one tube. A long total length of delay line can be used if the line is divided into sections with a driving tube after each section as shown in Fig. 8. We have constructed circuits having as many

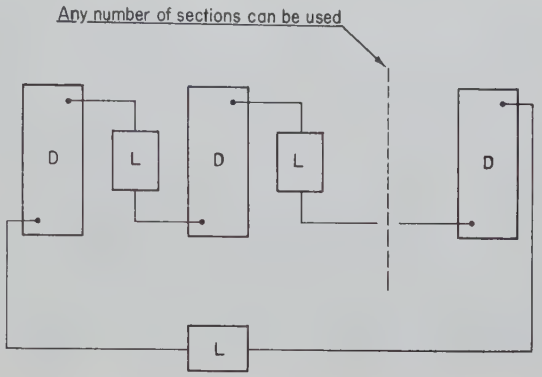

Fig. 8—Block diagram of system which can be used to extend the lower frequency limit of a pulse generator. This system can also be used to extend the storage capacity of a memory circuit.

as six EFP-60 tubes and an over-all prf of 710 kc. This lower limit was imposed only by the amount of cable we had available. With such a multiple driving tube circuit one can, of course, have a number of points at which pulses can be introduced to or taken from the circuit.

Any reduction in the actual amount of cable used will be of a practical advantage. One manner in which this can be accomplished is to use the delay line in such a way that the pulse travels twice the length of the line during a recycling period. Fig. 9 shows one such circuit. The cable length corresponds to 0.25 μsec whereas the total delay time is 0.5 μsec since the pulse is reflected in phase from the end of the cable and travels back to the plate and cathode to complete the period. This particular circuit was designed only to test this type of operation and improvements could probably be made.

Various mixing operations can be performed with these types of recycling circuits. A low-frequency, small amplitude modulation can be applied at the grid or other normally quiescent points of the tube without disturbing the recycling operation. A clock signal can be applied at the grid which will allow the recycling to occur only at a particular frequency, provided the clock frequency has the correct relation to the frequency determined by the length of the delay line. A varying prf can be obtained by connecting the dynodes of two or more different circuits as a common output. The prf will

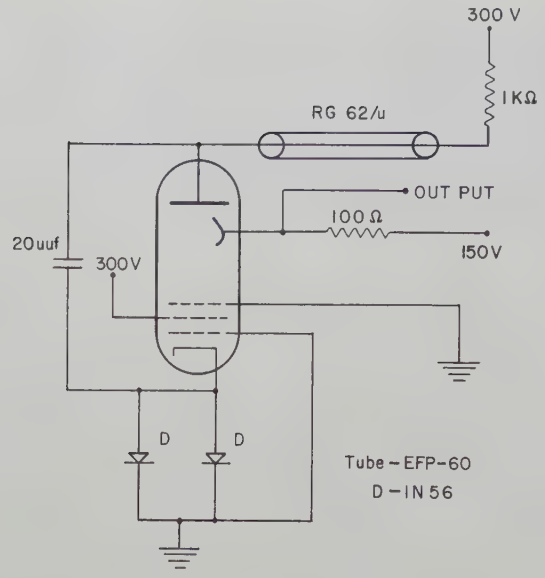

Fig. 9—Recycling circuit which doubles the effective time length of the delay line

then vary between one whose period is of the order of the pulse width and one whose period corresponds to the shortest delay line provided the lines are not integral multiples of each other. As the distance between pulses approaches the pulse width the output pulse from the dynode will be some combination of the two pulses with respect to amplitude and width.

Recycling systems, which operate by feeding back the dynode signal to the control grid, have been constructed but there are objections to this type of operation. In such a system, triggering signals must be applied to the cathode, requiring a large amount of power since the cathode has a low-input impedance. There is also no advantage to be gained since the principal output load for both systems is the delay line.

Discussion

Circuits for pulse generation and high-speed storage have been devised which are analogous to the mercury delay-line circuits but which operate at frequencies higher by at least an order of magnitude. The use of secondary emission tubes provides additional features because of the output available at the dynode. A rough measurement of the frequency stability of the recycling circuits was made and it appears that the stability is at least as good as that of a system using a mercury delay line.

The principal disadvantage to this system is the physical bulk of the delay cable. If, however, this system is compared with others on the basis of amount of information stored per unit time then the higher storage density possible with the delay cable partially offsets the objection to its physical size. An appreciable reduction of this physical size does not seem possible if coaxial cable is used but the use of microstrip transmission lines might offer some possibilities. If lower frequencies and longer pulses can be tolerated the size can be greatly reduced by using a lumped constant delay line. An indirect method of reducing the physical size could be achieved if a driving tube were available which could generate shorter pulses of sufficient amplitude. The same number of pulses could then be stored in a shorter length of delay line. This would require a tube with a smaller input and output capacitance and having a steeper characteristic than that of the EFP-60. The greatest storage density is, of course, obtained with a system of the type shown in Fig. 8 comprised of circuits of the type shown in Fig. 7.

Both the pulse generator and memory circuits have been used in our laboratory as adjuncts to other equipment. The authors have also built complete memory systems from these circuits. The operation of the circuits is very reliable and, as can be seen from the types mentioned in this paper, the basic circuit is quite versatile.

Acknowledgment

The authors acknowledge the assistance of Reinhold Gerharz, Laszlo Monostori, and Geoffrey Uyehara in the construction and testing of the experimental circuits shown in this paper and the help of Mrs. Susan Finnell Hart and Miss Ruth E. Berryman in the preparation of the manuscript.

The IBM 705 EDPM Memory System*

RICHARD E. MERWIN†

Summary—The IBM 705 memory system utilizes magnetic cores both as a storage element and also in a matrix address selection system. The magnetic core has been established as a memory element for large data processing machines. The core compares very favorably with other means of storage with respect to such factors as speed, reliability, size, cost, life, and simplicity of associated electronic circuitry.

The memory consists of a main 20,000 character unit and a 512 character storage unit. Both are three-dimension coincident current systems with the larger containing 35 planes of 4000 cores each and the other consisting of seven planes of 512 cores each. The basic memory cycle is 9 μs long when operating with the input-output units or on internal transfer of data. When operating with the central processing unit a 17-μs cycle is required. Data may be transferred within memory in five character blocks, and the five character instructions are transmitted to the control unit in one-memory cycle. Transfers between memory and the input-output and arithmetic units is serial by character.

Use of the magnetic core matrix switch greatly reduces the electronic equipment required to drive the memory. Simplified circuitry requiring no adjustments eliminates any maintenance time required for making routine adjustments. Indefinite life of the core eliminates any replacement problem of the basic storage element itself.

THE IBM 705 is a large scale data processing machine designed for commercial applications. It consists of a central processing unit which performs arithmetic and logical operations on business data at very high speed, auxiliary data storage in the form of magnetic tapes and drums, and input-output media which include punched-card equipment and line printers. Within the central processing unit there is a large rapid access memory unit which can be addressed at random. In addition, sixteen small logical storage units are provided to serve as accumulator registers for the arithmetic unit. This paper will describe the logical system and circuitry of this equipment in which the magnetic core is used as the storage medium.

The use of the magnetic core as the storage element in the 705 was motivated by a number of factors such as speed, reliability, size, and simplicity of associated circuitry. Because of the nonvolatile nature of magnetic storage, no equipment or time is required for regenerating the memory system. In addition to the time advantage, the problem of repeated references to one area of memory is eliminated.

The character is the basic unit of information in the 705 system and consists of six bits plus a redundancy check bit. The large scale memory has a capacity of 20,000 characters stored in 35 planes of 4000 magnetic cores in a 50×80 matrix. A 705 memory plane is shown in Fig. 1.

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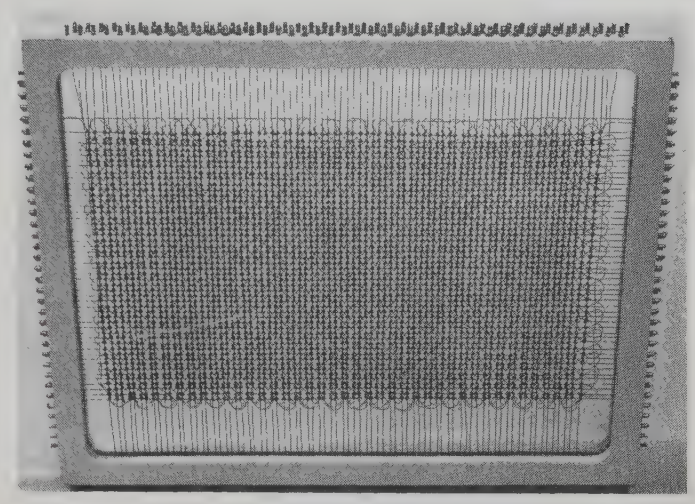

Fig. 1—The 705 memory plane.

The sixteen logical storage units are contained in one array consisting of seven planes. Each plane is a 16×32 matrix, thereby making the total capacity of this array equal to 512 characters. The array is subdivided into one unit having a capacity of 256 characters, a second unit of 32 characters, and 14 smaller units of 16 characters each.

Data flow in the 705 is serial by character on seven channels with the two exceptions noted below. Input-output information enters the CPU (central processing unit) via CR2 (character register #2) and then goes through the ALU (arithmetic and logical unit) and into memory. Data leaving the CPU for the input-output units come from memory via CR1 (character register #1). Internal arithmetic and logical operations call for a character from the memory and storage units via CR1 and CR2 respectively. The result of the arithmetic or logical operation is returned to the specified storage unit or in the case of some logical instructions (*i.e.*, add to memory, store, etc.) the result goes back to memory. A simplified block diagram illustrating the information flow is shown in Fig. 2.

The basic memory cycle is 9 μsec long, consisting first of a 5-μsec read period during which the information is read out of the cores. The remaining 4-μsec write period is used for entering data back in to the memory. When operating with ALU, another 8 μsec is required between the read and write periods for the arithmetic and logical operation, giving a total cycle time of 17 μsec. When executing input-output instructions and transferring data internally in memory, the basic 9-μsec cycle is used; for all other instructions the 17-μsec cycle is required.

The two exceptions to the serial by character flow of data in the 705 are reading of instructions out of mem-

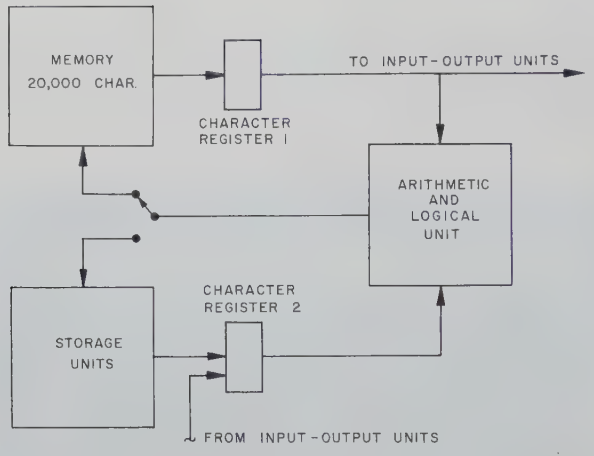

Fig. 2—Data flow in the 705.

ory, and the internal transfer of records within memory which can be accomplished at a rate of five characters per machine cycle. Instructions are five characters long; one for the operation code and four for the address. By virtue of parallel read-out it is possible to read an instruction out of memory in one character cycle. Transfer of records within the memory in five character blocks requires two 9-μsec cycles. The first of these cycles is used to read five characters into the memory buffer register (described later) and during the second cycle, the information is written into the new memory location.

Description of the Memory System

The operation of this type of memory array has been adequately described,[1–6] so no further description of its operation need be given here.

During the read part of the memory cycle, five characters from the core array are stored in a set of triggers, one associated with each plane, referred to as the memory buffer register. Because read-out of magnetic cores is destructive, information to be returned to memory must be retained in this register until the following write part of the cycle. New information to be entered into the memory is gated directly to the inhibit drivers.

A 705 memory cycle is initiated by setting the address of the required character into the memory address select register. The address consists of four decimal digits plus a single bit position which specifies the first or second ten thousand addresses in the memory. A diode matrix is used to decode the address into four output lines which drive the magnetic core matrix switches to be described below. A further selection is made of the desired character from among the five selected and read-out of the array. This is accomplished by another diode decoding matrix attached to the memory address register. The output of this matrix controls the memory output switching circuits which permit only the addressed character to be transmitted from the memory buffer register to the ALU. A block diagram of the memory and storage units is shown in Figs. 3 and 4 respectively.

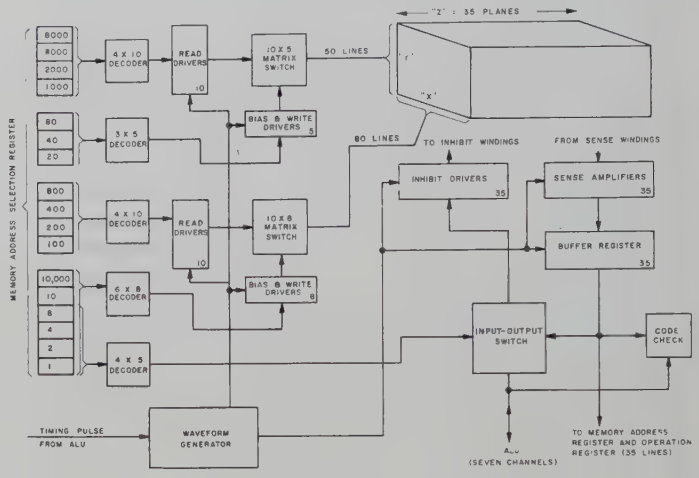

Fig. 3—705 Memory system block diagram.

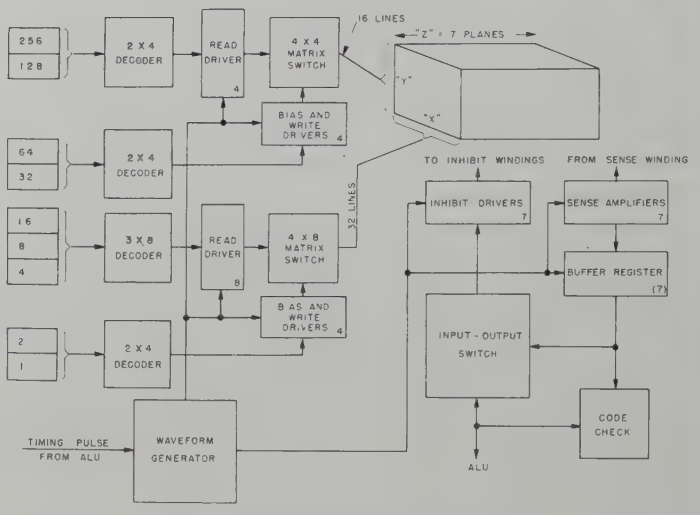

Fig. 4—705 Storage system block diagram.

The Matrix Switch

An important feature of the 705 memory system is the use of a matrix switch to provide both the X and Y selection currents. The current pulses for the 80 X lines come from an 8×10 switch and a 5×10 switch drives the 50 Y lines. The switches consist of pulse transformers utilizing a 4-79 Molybdenum Permalloy tape core with a rectangular hysteresis loop as shown in Fig. 5. A schematic of the transformer showing the three windings is given in Fig. 6. An anticoincident system of selection is used in the switch, so that by specifying one

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[2] Jan Rajchman, "Static magnetic matrix memory and switching circuits," *RCA Rev.*, vol. 13, pp. 183–201; June, 1952.
[3] William N. Papian, "A coincident-current magnetic memory for the storage of digital information." Proc. IRE, vol. 40, pp. 475–478; April, 1952.
[4] Jan Rajchman, "A myriabit magnetic-core matrix memory," Proc. IRE, vol. 41, pp. 1407–1421; October, 1953.
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[6] M. A. Alexander, M. Rosenberg, and R. Stuart Williams, "Ferrite core memory is fast and reliable," *Electronics*, vol. 29, pp. 158–161; February, 1956.

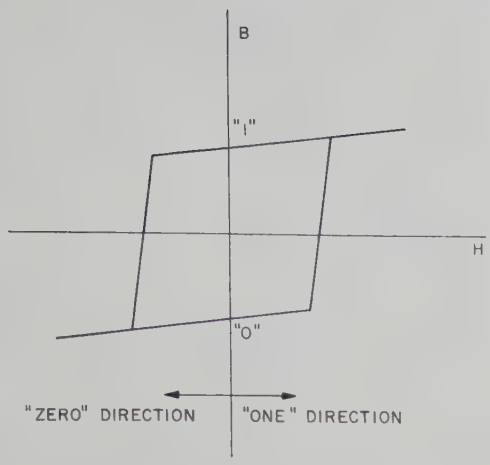

Fig. 5—B-H Plot for switch core.

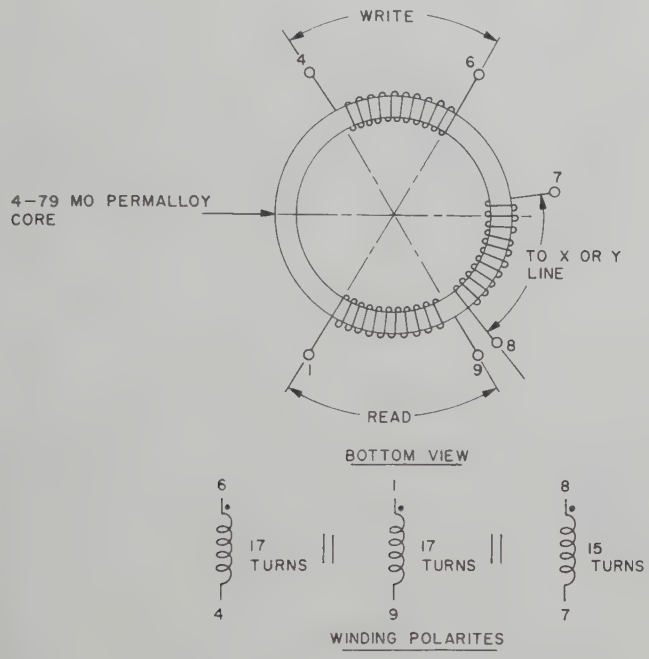

Fig. 6—Matrix switch transformer.

coordinate on each dimension of the matrix, just one pulse transformer emits a current pulse to its associated X or Y line. A schematic of the switch is shown in Fig. 7.

All cores in the switch are initially set to a "zero" state of magnetization and at the beginning of the read part of the cycle, a current is sent along all lines except the selected line on the read bias and write side of the switch. This biases all the cores on these lines in the "zero" direction. A current along the selected line on the read side of the switch sets the one core on this line not already biased off to the "one" position. The flux change during the transition produces an output current for the associated X or Y line. This completes the read part of the cycle and one core in the matrix is left in the "one" state of magnetization.

During the write part of the cycle the switches must generate a current pulse in the same X and Y lines as in the read part of the cycle but in the opposite direction. The two switch cores, previously set to "one" will produce the required current when reset to "zero." This is done by sending a current pulse along the previously unselected line on the read bias and write side of the switch in the same direction as the current pulse used to bias off the other lines on that side during the read part of the cycle. This resets the previously selected cores to "zero" which generates the required write pulse in the same X and Y lines selected during the read part of the cycle.

The main advantage of using the matrix switch to drive the memory selection lines is the reduction in required current drivers. In general the dimensions of the matrix are the two largest integral divisors of the total number of lines driven by the switch. In the 705 this amounts to 33 current drivers required for the matrix switches as compared to 130 drivers required if direct X and Y line drive was used. The choice of anticoincident logic in the matrix switch reduces the number of windings required for each switch core and reduces the power dissipation in the switch.

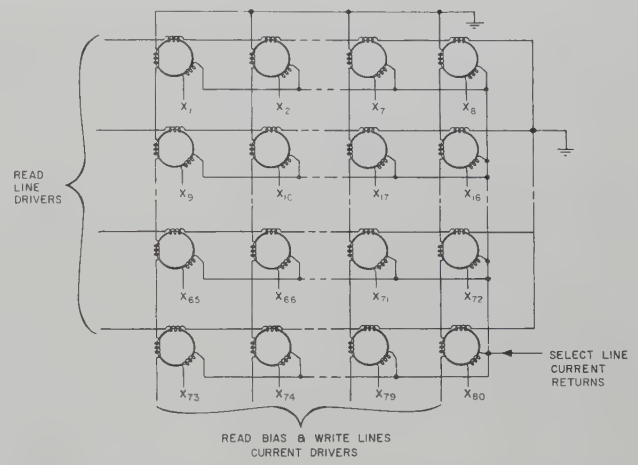

Fig. 7—Matrix switch.

The Current Driver

A vacuum-tube feedback amplifier is used to generate the current pulses required in the switches and the plane inhibit winding. A schematic of this amplifier is shown in Fig. 8. The input required to turn on the current driver is a positive machine pulse starting from minus 25 volts up to plus 10 volts with a rise time of about 0.5 μsec. This input causes the current flowing through the ground clamp diode to flow through the reference pulse generator tube (V_1) developing an accurate amplitude pulse across the 3.5-k resistor in the plate circuit. This negative pulse of 21.5 volts amplitude changes the reference voltage of the input stage (V_2) of the feedback amplifier which causes current to flow in the driver tube. This current will build up until the voltage across the 50 ohm resistor in series with the driver tube and the load equals about 20 volts which being fed back to

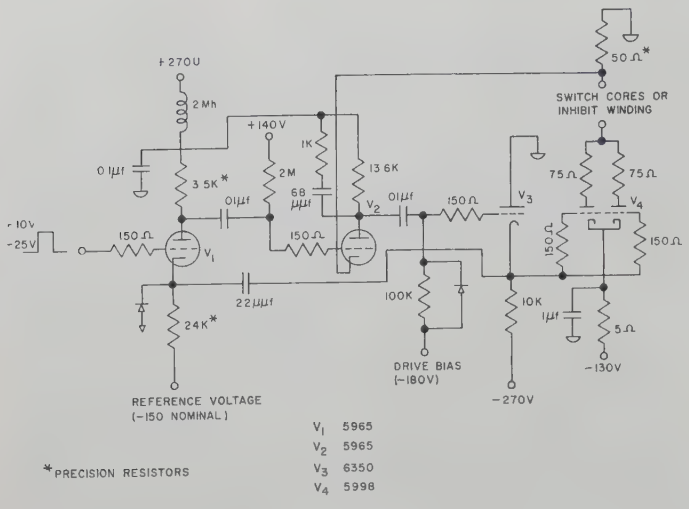

Fig. 8—Current driver.

the cathode of the input stage of the feedback amplifier establishes an equilibrium condition.

The degree of precision of the amplitude of the current pulse is determined largely by the cathode and plate resistors of the reference pulse generator and the 50-ohm resistor in the driver circuit. The former resistors are 0.5 per cent tolerance and the latter resistor is a 1 per cent unit. The use of some precision components and a feedback amplifier minimizes the effect of tube and component variations and provides current pulses with a high degree of uniformity.

By varying the return voltage of the cathode resistor in the reference pulse generator the current pulse amplitude may be varied. It is normal practice to use this voltage as a means for varying the drive currents in the memory selection lines. The selection current range over which the memory will continue to operate reliably is required to be plus and minus 8 per cent of nominal value when the X and Y currents are varied simultaneously.

The Sense Amplifier

The sense winding in each plane is connected to an amplifier which brings the "one" output voltage pulse up to a high enough level to gate "on" the associated memory buffer register trigger. The "one" output of a core has an amplitude in the order of 100 millivolts and is about 1.25 microseconds wide at the base. The "zero" output of a core has an amplitude of about 25 millivolts and peaks during the leading edge of the "one" output signal. Fig. 9 shows these two pulses superimposed.

The output of the plane is fed into a transformer which matches the low impedance sense winding into the higher input impedance of a vacuum tube and also provides some voltage amplification. Since the signals out of the plane are bipolar, it is necessary to rectify these signals to provide a unipolar output. This is done in the output of the transformer and then these signals

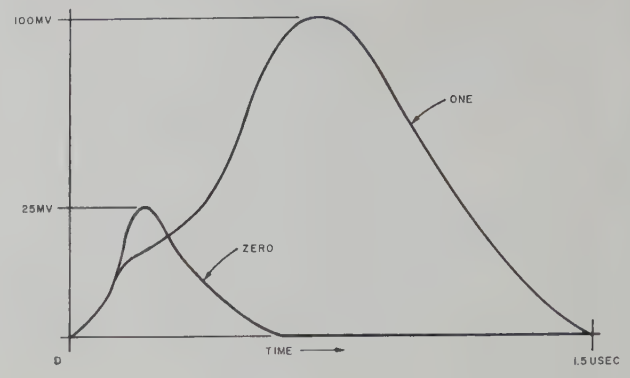

Fig. 9—Core output.

are fed into a two-stage pentode amplifier shown in Fig. 10. Some feedback is introduced into the amplifier by the un-bypassed cathode resistors in each stage.

During the turn-on of the "Z" axis inhibit drivers, large noise signals are generated in the sense winding due to magnetic coupling of the sense winding and the inhibit winding. These signals can block the amplifier making it inoperative during a subsequent read cycle. To prevent this a diode biased about one-half volt positive is used to clip out these signals at the input to the first stage of the amplifier.

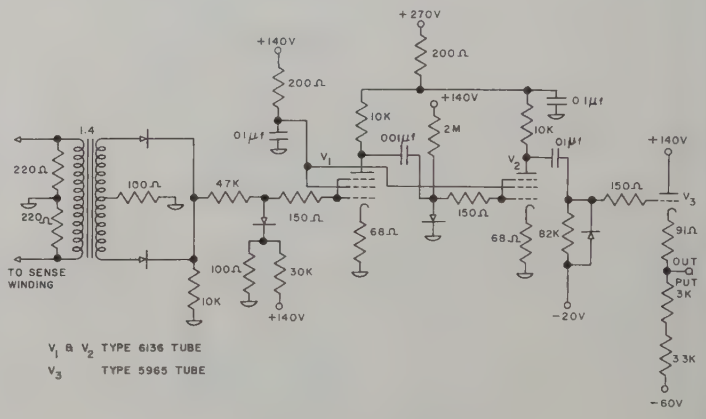

Fig. 10—Sense amplifier.

The input-output characteristics of a typical amplifier are shown in Fig. 11. It is of interest to note that the imperfect rectifying characteristics of germanium diodes at low voltage levels gives an attenuating effect at small signal inputs. This has the effect of masking out the zero signal from a core plane while a normal "one" signal is in the order of 50 to 60 volts at the cathode follower output. The amplifier output is sampled with a diode gate using a 0.5-μsec wide pulse into a memory buffer register trigger.

Input-Output Switching Circuits

The input-output switching circuits route the information selected in the memory to the input-output bus and route data for storage in the memory from the

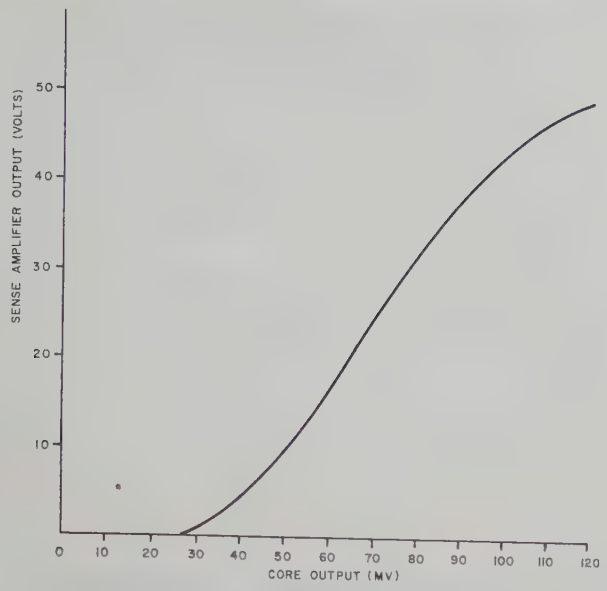

Fig. 11—Input-output characteristics of sense amplifier.

input lines. The control of this function is from the memory address register as described above. In the case of reading an instruction, all five characters are transmitted to ALU in parallel; this requires that all instructions be stored in memory at addresses modulo five. Writing into memory can only be accomplished one character at a time during a subsequent write cycle.

In all cases except instructions which store data in memory on the subsequent write part of the cycle, the inhibit drivers are switched to the memory buffer register except, as already noted, when the drivers for the specified character are fed from the memory "in" bus. The main difference between the storage and memory system is that no input-output switching is required for the storage units, since data are read out of the storage unit into CR2 and the result of the arithmetic operation is placed back in the storage units.

Special mention should be made of the "transmit" and "receive" instructions which enable the internal transfer of data within memory. Although single characters can be transmitted with these instructions, the most useful procedure is to transfer data in blocks of five characters—again requiring that the blocks be stored at addresses modulo five. The procedure is to give the "receive" instruction which specifies the address of the data to be transferred, and then follow this with a "transmit" instruction to locate the area in the memory where the data are to be stored. A series of two 9-μsec cycles as outlined above, follows until all the information is transferred.

Waveform Generator

The waveforms used in the memory are shown in Fig. 12. They are produced under control of the waveform generator which is driven by the 705 master clock. The bias currents for the switch come up early in the

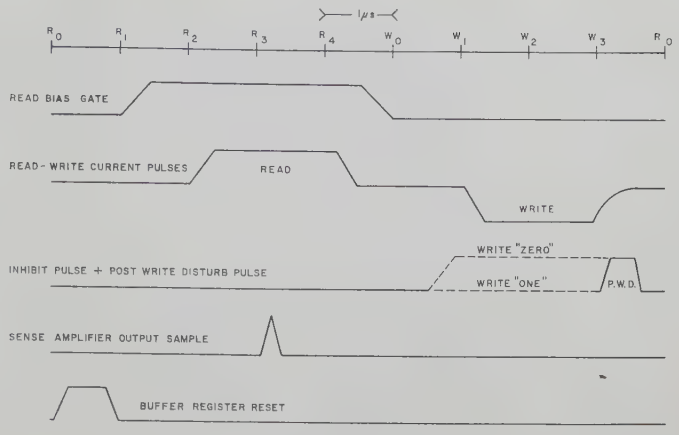

Fig. 12—Timing waveforms 705 memory.

read part of the cycle, followed about one μsec later by the read pulse sent along the selected X and Y lines. The read sample, which comes about 1 μsec after the read pulse, gates the "one" (if any) into the memory buffer register. Fall of the bias and read currents completes the read part of the cycle.

The initial step in the write part of the cycle is to bring up the inhibit current pulses and then the write pulse about one-half μsec later. After the fall of the write pulse a post-write disturb current is generated in the inhibit windings of all the planes to reduce the noise from unselected cores in subsequent read cycles.

The memory and storage units are contained in two frames and occupy 23 square feet of floor space. One frame contains 121 pluggable units while the other frame includes the core array and the current driver tubes. A total of 675 tubes consumes approximately 7.6 kw of power. A view of the memory frames with covers removed is shown in Fig. 13 with the core array on the left next to the current driver panels and the pluggable unit frame on the right.

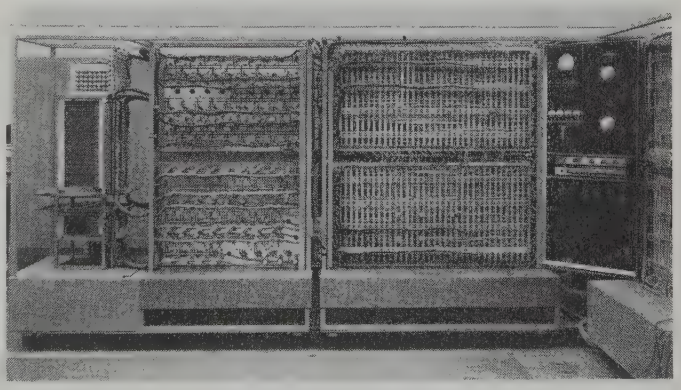

Fig. 13—Memory frame.

Acknowledgment

The author wishes to acknowledge the contributions made by P. E. Fox and other members of the IBM Product Development and Research Laboratories.

The AN/FSQ-7 Computer jointly developed by Lincoln Laboratory, Massachusetts Institute of Technology, and the Kingston Engineering Laboratory, International Business Machines Corporation, is a primary element in the SAGE air defense system. The following three papers, derived from this joint Lincoln-IBM program, present the philosophies and practices which were mutually evolved to achieve the operational reliability demanded.

The reliability requirement for continental air defense computing equipment is as stringent as has ever before been encountered. The requirement for this real-time application is virtually error-free, round-the-clock performance. This demands the achievement of a new high in equipment reliability and the establishment of a maintenance procedure which will yield continuous system performance.

To achieve satisfactory equipment reliability in a system comprised of more than sixty thousand vacuum tubes and more than one and a quarter million components, an intense component development and circuit design program is essential. Error-free performance while the equipment is in operation demands that all failures be predictable in nature and eliminated during periods of scheduled maintenance. The use of duplicate equipment provides the opportunity to perform scheduled maintenance without disruption of system operation.

The philosophies and techniques that evolved from the component development program, the circuit design program, and the marginal checking and maintenance program are presented in these papers.—*The Editor*

Reliability of an Air Defense Computing System: Component Development*

HAROLD F. HEATH, JR.†

Summary—**This paper presents the general aspects of the component development program for the AN/FSQ-7 Air Defense Computer. The requirements of the system for high reliability and long life necessitate proper selection of the type of component, proper specification of the component to the manufacturer, and proper component application by the circuit design engineer. The component development program has made free use of ideas from the computer industry and the component industry.**

Introduction

THE RELIABILITY of a high-speed electronic digital computer depends on many factors, among which is the performance of the electronic components which comprise the system. The purpose of this paper is to describe an electronic component reliability program which was initiated to provide electronic components which would satisfy the requirements of the air defense computer.

System Requirements

The type and quality of components which may be used in an electronic system depend, to a large extent, on the operational requirements of the system. In the present case there are two major system requirements which impose restrictions on the selection and use of electronic components. First, the system must operate continuously for long periods of time. The normal operational schedule is interrupted periodically for short routine maintenance periods which do not significantly alter the operational environment of the electronic components. The second system requirement is that catastrophic shutdown of equipment during the operational period must be minimized.

The first system requirement dictates that the average life expectancy of the individual components should be long, in fact, on the order of tens of thousands of hours. It is well known that existing electronic components, such as resistors, capacitors, diodes, and the like, are potentially capable of this type of service if operated within satisfactory environmental conditions and not subjected to operational abuse. Catastrophic failure of a component is defined as any sudden change of characteristic which might cause the computer to malfunction, assuming all other conditions to be normal. It is clear then, that the second system requirement dictates that catastrophic component failure be minimized. It requires that the short-time life characteristics of the components employed be predictable in the presence of normal operating conditions. From a component point of view, it implies that we must know and insure the mechanism of failure by suitable component methods which minimize or eliminate the occurrence of catastrophic failure. This second problem is of major consequence in the selection of suitable components to meet the requirements of the air defense computer.

The choice of suitable components depends, also, on the operational environment provided. In the present instance, the system is environmentally defined by controlled temperature and humidity; by low vibration which is typical of large ground computer installations; and by both dc and high-frequency pulse type computer circuit operation. The operational environment was designed to optimize component reliability in so far as was practicable.

Within the system there are two distinct levels of reliability. Those portions of the system which process digital data in such a manner that the loss of data is catastrophic to the performance of the system are considered to be of Level I reliability. Those portions of the system which process statistical information, or are of

* Manuscript received by the PGEC, March 5, 1956; revised manuscript received July 16, 1956.

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such a nature that the loss of small amounts of information are not catastrophic, or where the program can be repeated to provide the correct answer, are considered to be of Level II reliability. It was considered that Level II reliability requirements would be satisfied by the use of existing components which met established military specifications of performance. The bulk of the component program was aimed at providing components possessing the high degree of reliability required by Level I portions of the system. The balance of this paper will be concerned with this problem.

The Component Program

Briefly, the component requirements are for long life and predictable characteristics. Our existing commercial components do not possess, in general, all of the desired qualities. A certain quantity of them in any given system will exhibit random or nonpredictable catastrophic failures. The prime sources of trouble in applications of this nature in the past have proven to be vacuum tubes, germanium diodes, relays, and RLC type components in relative order to anticipated failure rate. Some idea of the nature of the problem at hand may be gathered from the fact that this system contains more than one million electronic components of the above types which will be expected to operate without experiencing catastrophic failures during the operational periods of the system. It should be noted again that the components will operate in pulse type circuits where each pulse may represent significant information; therefore, the generation of a random pulse by a mechanically, electrically, or thermally agitated component is construed as catastrophic and must be minimized. The major component problem was to select those component types which promised the highest degree of reliability and then to attempt to eliminate the underlying causes of random failure within each type.

Selection of Components

To select the proper types of components to be utilized in the system, an investigation was initiated which encompassed 1) many component manufactures, 2) many contemporary component reliability programs, and 3) component experience at M.I.T. and IBM. As a result of the extensive investigation, the available components were classified as follows: 1) certain components were adequate, 2) certain components were inadequate but could easily be improved to the required standard of reliability, 3) certain components were inadequate and would require extensive development by the component industry to meet the required standards, and 4) certain components were inadequate, and due to the nature of the system, could in all probability never be made adequate. Composition carbon resistors and common point-contact germanium diodes are among those components which were deemed entirely adequate for the system.

It was felt that paper capacitors, deposited carbon resistors, certain high-current germanium diodes, and many other components, could easily be improved by the manufacturer to meet the required standard of reliability. For example, there is some controversy concerning the construction of highly reliable paper capacitors. To assure the procurement of paper capacitors, all having a high level of reliability, it was deemed necessary to require that the dielectric specifically consist of three sheets of paper impregnated with pure mineral oil. This type of specification governing manufacturing processes and materials is essential to a high level of reliability and is extensively utilized in procurement specification.

Those components requiring extensive improvement or development were vacuum tubes, particular types of diodes, high-frequency pulse transformers and magnetic cores. For example, the standard vacuum tube has difficulties which are detrimental to digital data processing systems. These difficulties are: 1) cathode interface or "sleeping sickness," and 2) intermittent shorts. Both of these effects can be minimized only by action at the manufacturing level. This action was required if vacuum tubes were to be utilized in the system. As a result of the program undertaken to minimize these defects the resulting tube types available to industry are significantly improved in these and other respects.

Metallized paper capacitors, because of their "pulse-healing" effect, are an example of components which were deemed unsuitable for use in the system.

When the necessary groundwork had been completed, procurement specifications were written for all of the required components using existing military specifications as minimum requirements. Additional requirements placed on these components were specifically designed to eliminate from the statistical group those individuals which tended to have the highest probability of failure. These additional requirements were based on life testing of each lot of components and improved processing and selection methods. A basic precept in the formulation of all component specifications was that in processing manufacturing control of critical process steps is the only reasonable method to eliminate the minority group of unreliable components. It should be recognized here that the component manufacturer has played an important part in the preparation of the specifications; and, indeed, he has supplied much of the information required to prepare these sometimes extensive documents which deal so intimately with his manufacturing processes.

Use of Components

The selection and specification of components is not sufficient to guarantee high reliability. It is equally important that the components are used properly. It has already been stated that the temperature and humidity were fixed at levels consistent with long component life. It is also necessary to establish the proper electrical operating conditions if a common level of reliability is to be obtained. All of the information and experience available concerning the proposed use of these components was incorporated into a set of application rules which, when followed by the design engineer, would

insure a common level of reliability. The application data concerning each component were called component application memoranda and contained such information as: minimum and maximum electrical ratings, in what types of circuits the component could be used, and the time-dependent electrical characteristics of the component. The uses of the data by the design engineer are described in an accompanying paper. It is sufficient to say that the purpose of these memos was to minimize component application abuse.

A method frequently employed to obtain increased component reliability is derating of electrical power, voltage, and current. For example: 1) the maximum allowable power dissipation in a composition carbon resistor is 50 per cent of the commercial power rating; 2) the voltage rating of paper capacitors is 50 per cent of the commercial voltage rating; 3) the current and voltage ratings of selenium rectifiers is 75 per cent of the commercial ratings; 4) vacuum tube ratings are maintained within prescribed ratings, while the bulb temperature must not exceed 80°C. These are typical deratings employed in the air defense computer to optimize the operational reliability.

The essential characteristic of a component on which circuit operation is dependent is normally expected to vary with time. Types of time variation are: 1) catastrophic, 2) short term, and 3) long term. Catastrophic failures cannot be anticipated by the computer; hence, they must be eliminated by the component selection and specification technique. Short-term variations include such things as temperature and voltage coefficients and other influences which might cause a component parameter to change over a very short period of time. Long-term variations are those permanent changes which occur over a period of weeks, months, and years. Characteristic variations are detected by the marginal checking system which is explained in an accompanying paper.

A component margin is that variation from the "norm" of a specific characteristic which might be expected to occur during the life of the equipment (often called end-of-life tolerance). For example, the initial (purchase) resistance tolerance of composition carbon resistors is ± 5 per cent. The maximum voltage coefficient of resistance is -0.35 per cent/volt for $\frac{1}{2}$ watt sizes. The temperature coefficient is of little concern in a system at 25°C. ambient. A variation of ± 10 per cent in resistance is expected to be sufficient to encompass both short- and long-term changes in resistance. This expected variation is based on experience and life tests. The "component margin" is then specified as ± 15 per cent, and the circuit designer must design circuits with both the component margin and the purchase tolerance in mind. Other examples of purchase tolerance and component margin are given in Table I.

The method by which the circuit designer stays within these tolerances is explained in an accompanying paper. The circuit designer is responsible for maintaining each component within its electrical rating, in the midst of many parameter variations, over the life of the system. This contribution assures proper environmental operation of components, and the possible attainment of maximum reliability.

TABLE I

Component	Parameter	Purchase Tolerance	Component Margin
Precision film resistors	R	± 1 per cent	± 5 per cent
Paper capacitors	C	± 10 per cent	± 22 per cent
Germanium diodes	R_b	R_b (min)	$1/5\ R_b$ (min)
	R_f	R_f (max)	R_c (max)
Vacuum tubes	I_b	Varies	$+25$ per cent -50 per cent

Other Aspects

In addition to the program designed to select and use components judiciously, procedures were established in the assembly process to safeguard the reliability of the components involved. Rough mechanical usage and improper soldering techniques are deleterious to component life. Wherever possible, it is desirable to carry out the assembly process with automatic techniques. It is anticipated that the automation of production processes will help to solve many of the problems. However, any system of production will lead to the destruction of a small number of components; hence, it is necessary to inspect each completed subassembly prior to its assembly into the system. This is done on a rigorous basis utilizing test criteria which simulate actual operation in the system.

An extensive program of life testing electronic components was necessary in order to establish some of the data required by the design engineers and to determine the level of reliability of the newly developed components. In addition to the life test program, a systems analysis program is being used to evaluate the entire component program. This analysis program is based on a punched card system which will be of aid in the statistical analysis of component failures.

Conclusion

This program was an attempt to derive a special class of electronic components defined by a requirement for ultrahigh reliability in an optimum computer environment. Initial systems analysis tests have indicated that most of the initial component goals have been achieved. In those instances where the components have been found wanting, the path toward higher reliability has been well established. This high reliability can only be a product of a joint effort of all concerned. Component manufacturer, component engineer, designer, manufacturing engineer, and systems engineer, are prominent among those responsible for the reliable operation of electronic components in a data processing system. A continuing program of development in this area has been assured and promises to raise the standard of reliability for the electronic computer industry.

Reliability of an Air Defense Computing System: Circuit Design*

RAYMOND E. NIENBURG†

Summary—**Extreme reliability resulting in no unscheduled downtime and a low ratio of scheduled maintenance to operate time was the objective of the AN/FSQ-7 design program. The circuit design philosophy of this program is presented. In addition, an approach is given whereby the concept of marginal checking is applied to determine quantitatively 1) the relative reliability of computer circuits and 2) that a margin of safety consistent with the circuit design philosophy existed. An Appendix is included setting forth actual examples in a qualitative manner.**

THE PRECEDING PAPER discusses the program set up to obtain reliable components for the circuits of the AN/FSQ-7 computer. This component development program must be followed by a circuit design procedure which takes into account the ratings and tolerances of the components. Basic work on reliable circuits for a computer of this type has been carried out at the Digital Computer Laboratory and Lincoln Laboratory of M.I.T.[1-3]

The computer circuit designer, whose goal is thousands of hours of trouble-free operation plus a timely warning when circuit failure is imminent, faces problems quite dissimilar to those of, say, a missile control designer, whose goal is completely trouble-free operation for a short time after a relatively long period of shelf life. The design philosophies followed on this computer are presented here.

Component Considerations

The design of most circuits employed in a digital computer would be a relatively easy task if all components could be purchased within 1 per cent of the design value and if they remained unchanged thereafter. Since this is not presently possible, the main issues confronting the circuit designer in his quest for reliability revolve about the question of component tolerances.

There are three basic contributions to the total deviation from the purchased value.

Initial Variation

Generally defined in a specification written for purchasing components and referred to in the following text as initial purchase specification variation, *e.g.*, ± 5 per cent for composition carbon resistors.

Short-Term Drift

Many components exhibit a random fluctuation around some "norm." This fluctuation is a smaller percentage variation than initial variation and includes environmental variations introduced by the voltage, temperature, and humidity coefficients inherent in most components.

Long-Term Drift

The result of gradual deterioration of the component resulting in eventual failure. The value of the component at the failure point and hence the limiting value of the long term drift is defined as the end-of-life value. The allowable limits on long-term drift are generally a matter of component experience and are based on an attempt to realize a useful life consistent with all other components in the system. A balance must also be sought between the amount of deviation permitted and cost, in terms of numbers of components and replacement difficulty.

The problem encountered by the circuit designer is, therefore, to establish and live within a consistent philosophy that will result in highly reliable circuits utilizing components that are reproducible only within limits and that are unstable as well.

Catastrophic Failures

The catastrophic failure of components has been discussed in the preceding paper. While there is little a circuit designer can do to eliminate this problem, it is often possible to insure that circuit failure resulting from the catastrophic failure of one of its components will not result in either a free-running circuit or in damage to neighboring circuits. Regenerative circuits represent the most serious threat because of their tendency to free run. By anticipating catastrophic failure of the critical components, blocking oscillators, single-shot multivibrators, etc., can be so designed as to become completely inoperative upon failure of these components. It is always possible to imagine a set of circumstances involving failure of components and voltages that lead to free running, but it is also possible to minimize greatly the chances of creating chaos in information paths.

The elimination of cascading failures is generally more straightforward. Take, for example, the simple case of a cathode follower returned to a high negative

* Manuscript received by the PGEC, March 5, 1956; revised manuscript received, July 16, 1956.

† Internatl. Business Machines Corp., Kingston, N.Y.

[1] N. H. Taylor, "Rudiments of Good Circuit Design," Digital Comp. Lab. Rep. R-224, Mass. Inst. of Tech., Cambridge, Mass.; May 19, 1953. Presented at the Electronic Components Symposium, Pasadena, Calif.; April 30, 1953.

[2] N. H. Taylor, "Designing for Reliability," Lincoln Lab., Tech. Rep. No. 102, M.I.T.; December 9, 1955.

[3] J. W. Forrester, "Design and Tests of Electronic Circuits for Operating Safety Margins," Div. 6 Memo. M-1828, Lincoln Lab., M.I.T.; January 27, 1953.

voltage driving one input of an "OR" circuit as shown in Fig. 1. Any failure causing loss of cathode follower current (*e.g.*, loss of plate voltage, filament voltage, internal tube short, large negative grid excursion, etc.) will place a reverse voltage of approximately $-V$ across D_1 which may be excessive and result in diode failure. The simple expedient of a clamp or protection diode (shown dotted) eliminates the danger to D_1 thereby limiting failure to the cathode follower. Listing the effect of the failure of each component generally makes potential trouble spots obvious.

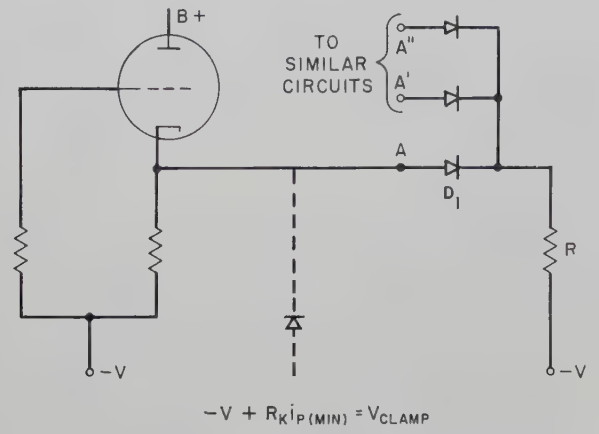


Fig. 1—Addition of clamp diode illustrating the elimination of cascading failure in the event of tube failure.

Design Philosophy

Normal operation is expected from a circuit comprised of randomly selected, "in-spec" components. A circuit must be shown also to be capable of meeting all its operating specifications with margins under the conditions that each component is "off" from the design center value by the initial purchase limit in a direction calculated to result in the worst possible tolerance build-up. In other words, a circuit made with shelf components must function properly and have some life expectancy.

Furthermore, to provide a quantitative measurement of the operating margin remaining, the most critical component (usually the tube) was allowed to deteriorate to its end-of-life limits, again in the worst direction, and demand that the circuit at least *meet* all input-output specifications. Thus, every circuit must meet all of its performance specifications when constructed using components that have deteriorated to the following extent: the component judged to have the most critical effect on circuit performance will be at end-of-life (see the part on "Long Term Drift" above), and all other components will be at the extremes of their initial purchase "specs" (see the part on "Initial Variation") in a direction calculated to have the worst cumulative effect.

Marginal Checking

The implication was made earlier that to meet one of our design objectives, all circuit failures must be predictable. Again relegating the problem of catastrophic failures as belonging exclusively to the components engineer, let us examine a means, called marginal checking, of predicting failures caused by drifting components.

Basically what is required is a convenient means of aggravating, by simulating the passage of time, any condition created by component drift which, before the next scheduled maintenance period, will cause failure. The most convenient variable to accomplish this simulation appears to be a supply voltage. The selection of a supply voltage permits remote selection, automatic checking, the most rapid isolation of failure, and the important feature of being able to restore the system to its original state simply if reasonable caution is taken not to use excessive excursions. Hence, if it can be shown that a supply voltage variation can satisfactorily simulate the effect of component deterioration on circuit performance, the need for a marginal checking variable will be met. This has been demonstrated experimentally.[4] Considerable ingenuity is often required, however, to select the proper voltage for use as the marginal check line 1) to insure detection of deterioration of *every* component and 2) to result in as few variable supply lines as possible. Since each type of circuit presents a unique challenge, a brief examination of a few specific circuits may be more illustrative than a general discussion. Several examples have been set forth in an Appendix.

Design Marginal Checking

Examination of marginal checking data indicates that, besides a tool for the prevention of system difficulties, marginal checking may also be employed to excellent advantage as a design tool. Marginal checking diagrams represent a quantitative method of comparing the relative reliability of similar circuits. After a marginal check line has been selected by demonstrating that the limits of its variation (*i.e.*, its margins) are a function of the components under scrutiny, curves are plotted of the loci of circuit failure vs this voltage for each component in question. Two things are accomplished: 1) the permissible tolerance of each component is known as a function of the marginal check voltage, and 2) the position of the operating point relative to the complete operating region is known. The effect of any design change can now be evaluated by comparing the limits of variation of the marginal check voltage. For this to be meaningful a complete definition of failure including the predeter-

[4] N. H. Taylor, "Marginal checking as an aid to computer reliability," Proc. IRE, vol. 38, pp. 1418–1421; December, 1950.

mined dissipation limits of all components is necessary. For example, if in a specific circuit the parameters of interest included:

Input	Ouptut
Input Signal Amplitude Repetition Rate	Rise Time Output Levels Pulse Width

then the design marginal checking curves would include plots of the loci of circuit failure, as defined by the input-output specifications, for every component in the circuit. A hypothetical result for one component is shown in Fig. 2. By observing the effect on these curves of variations in circuit design, a completely quantitative comparison between two designs can be made.

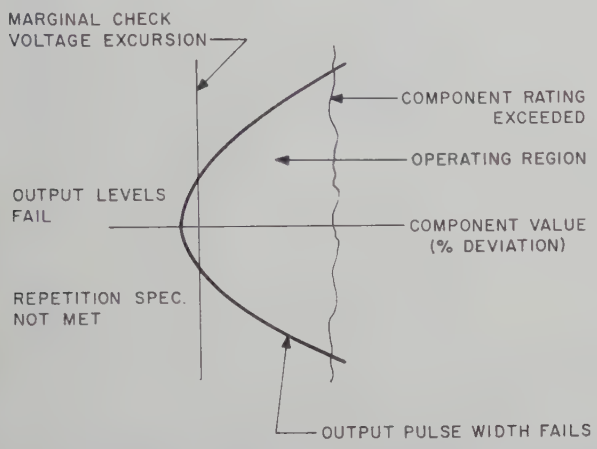


Fig. 2—Hypothetical marginal check curve depicting boundaries of operating region and specification violated in each region.

The reason for failure for each region is often significant and should always be recorded. In this particular curve it is apparent that an increase in the design value of the component under scrutiny will result in a better centering of the operating point. Since time (*i.e.*, component life) is the important parameter, however, a geometric centering may not be the optimum condition. Some components invariably display long-term drift in one direction. The values, therefore, should be so chosen that the margin in the direction opposite to the prevailing direction should be no greater than is necessary to account for initial and short-term variations. Also the condition often exists where the shift of one component will adversely affect a more critical component. Examination of a complete set of marginal check curves will indicate if the need for a shift in operating loci is beneficial.

Sudden Failure and Masking

Fig. 3 shows the results of a poor choice of a marginal check line. As the component value is decreased, instead of a failure loci of finite slope, the permissible ex-

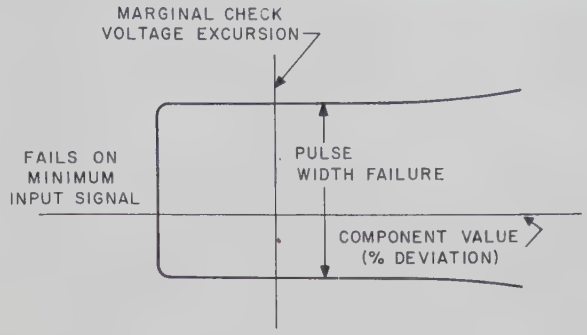


Fig. 3—Unsatisfactory marginal check curve indicating the need for a different marginal check voltage. Prediction of failure due to negative component deviation is impossible.

cursion of the marginal check voltage suddenly collapses to zero. Variations of this voltage, therefore, do not give any indication of imminent failure which would result from a negative drift in the value of the component under test. A marginal checking curve must approach circuit failure with a slope sufficiently small to permit detection of an impending failure at least one maintenance period prior to actual failure. Fig. 4 illustrates this basic requirement. Since it is necessary to have *every* failure predictable, a different (or additional) voltage must be selected to predict the failure of whatever component is under test in Fig. 3.

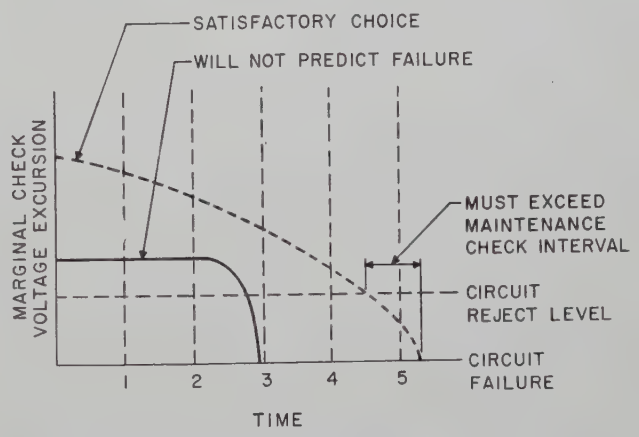


Fig. 4—Relationship of marginal check curves and length of maintenance periods. Failures are predictable only if at least one maintenance period exists between deterioration to reject level and failure level.

It can be seen from this discussion that the marginal check data also provide a cross check on the validity of the designer's selection of the marginal checking voltage.

Results

The techniques and philosophies presented here evolved and were followed in a program resulting in an extremely large, real-time computer. To provide the type of reliability demanded by the application, the tolerance placed on components (a partial list is presented in Table I) was quite wide.

TABLE I

Component	Initial Purchase Spec.	End of Life Deviation
Carbon Resistor	± 5 per cent	±15 per cent
Precision Resistor	± 1 per cent	± 5 per cent
Inductor	± 5 per cent	
Small Capacitor (Mica, Ceramic, etc.)	± 5 per cent	±15 per cent
Paper Capacitor	±10 per cent	±22 per cent
		±25 per cent
Tube		−40 per cent of g_m or i_p

These tolerances, employed in a manner consistent with the rule in the section on "Design Philosophy," resulted in a computer that gave very little trouble during assembly and now gives every indication of being unusually reliable.

While the expense in man-hours of completely marginal checking every circuit in a computer sometimes appears prohibitive, there are several compensating factors. The trend toward using basic building blocks throughout a system justifies a more concerted effort on this reduced number of circuits. Also the thorough understanding of each circuit that results from such a program eliminates much difficulty during assembly and frame test, and thereby effects a tremendous time saving. Furthermore, a degree of reliability is made realizable without demanding unreasonable stability or reproducibility from components.

Appendix

The selection of marginal-check-voltage lines must be made with great care to prevent an excessive number of them. Ideally, what is desired is a single voltage for each circuit that can be used to predict circuit failure. The variations of this voltage to produce circuit failure must be a continuous function of the value of every component in the circuit. Generally, the independence of a screen grid supply in pentode circuits makes it a natural selection. This is especially true in dc-coupled circuits where variations of the other supplies upset the divider networks and very effectively mask component variations. Feedback circuits are troublesome since a well-designed feedback circuit is constantly compensating for the mcv[5] variation. Quite often it is expeditious to break the feedback loop during circuit testing.

Because of the great diversity of circuit design, general rules for mcv selection are difficult to formulate. Rather than analyze a variety of circuits, some detailed results will be discussed to explain better the function of the mcv, thereby illustrating its selection.

Marginal Checking a Pentode Pulse Amplifier

The use of filament voltage as a marginal checking line was abandoned as impractical. Since emission varies sharply when the temperature limited region is approached, control, and hence repeatable data, are extremely difficult to obtain. With pentodes, plate voltage has relatively little effect on plate current past the knee of the plate characteristics. Screen voltage variations, however, simulate quite closely the effect of a deteriorating tube. When employed as a marginal checking voltage, the screen voltage has the advantage that since it is rarely in any feedback loops, its variations do not disturb divider returns. With pentode circuits it is generally the most convenient terminal for obtaining marginal check data.

Fig. 5 shows a typical pulse amplifier.

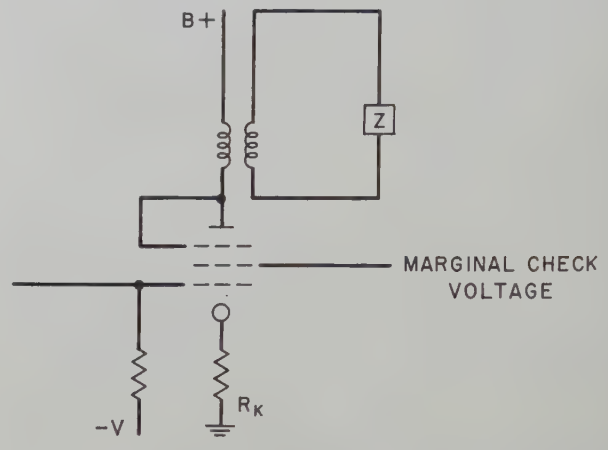


Fig. 5—Typical pulse amplifier.

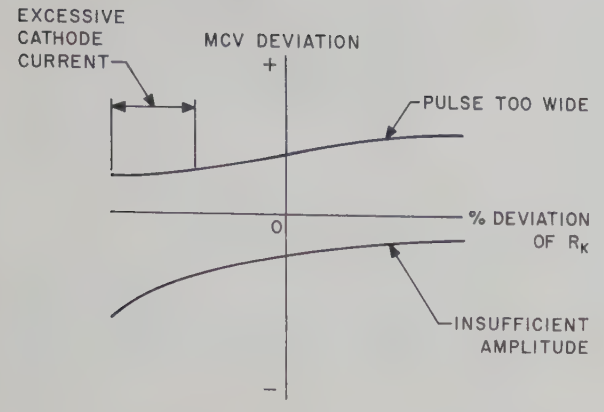
Fig. 6(a) is the marginal checking curve for the cathode resistor. A similar curve could be plotted for the transformer to assist in the selection of a turns ratio (design marginal checking) but since the characteristics of a transformer are comparatively stable, this information would not assist in predicting computer errors.

The only other component, the tube, represents a problem. To most conveniently simulate a deteriorating tube, the screen grid is varied. Since this is the marginal check voltage, however, we have only one variable, the screen voltage, to plot simulated tube condition vs marginal check voltage. Another type presentation of this information removes the difficulty. Fig. 6(b) shows the effect on output of a deteriorating tube as simulated by screen voltage variations.

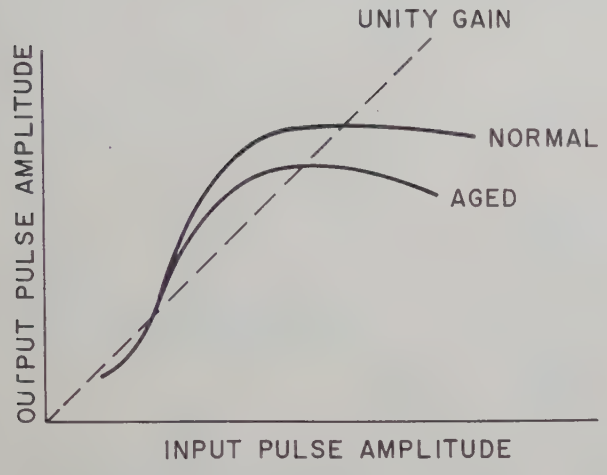
Selection of Marginal Check Line

Fig. 7 is a schematic of an ordinary bistable trigger circuit, or flip-flop. (The input has been omitted.) The circuit has three voltage supply points that may be inspected for marginal check lines; the plate supply, the grid-divider return, and the cathode return. As with any circuit employing a significant degree of cathode degeneration, this flip-flop is relatively insensitive to voltage supply variations if the variation does not upset the flip-flop balance. If either grid-return is varied with respect to the other, however, conditions necessary for bistable operation will soon be violated and circuit failure will result. It is reasonable therefore to select as a first choice for the mcv either of the plate supply volt-

[5] MCV—marginal check voltage.



(a)



(b)

Fig. 6—(a) Marginal check curve for R_k of Fig. 5; (b) Transfer characteristic of pulse amplifier showing effect of simulated tube aging.

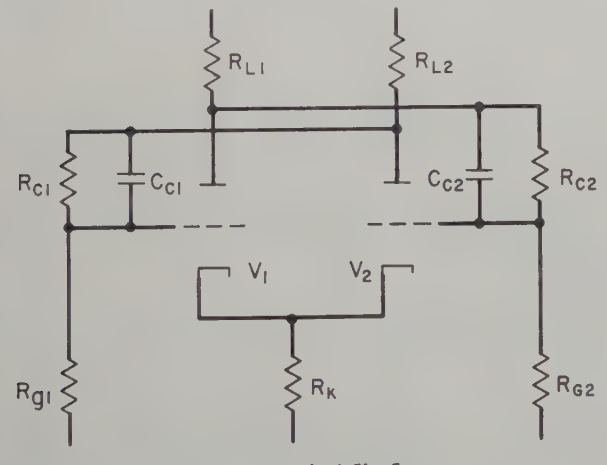


Fig. 7—Typical flip-flop.

ages or either of the grid returns. If a grid return is chosen, the circuit will certainly become unbalanced and fail to count as the voltage is varied significantly from its nominal value. The limits of the excursion before failure will clearly be affected by changes of any one of the divider resistors since the unbalance will either be aggravated or alleviated depending on the direction of the component change.

The plate resistors affect the magnitude of the grid swing. Since the operating range of grid voltages is a function of the grid-return voltage, the variations of plate resistors will also affect the limits of the mcv excursion.

This analysis can be continued to include all the components indicating that the grid-return supply fulfills the requirements of a marginal check line; *i.e.*, all component variations are reflected in the permissible excursion limits of the marginal check line.

Marginal Check Data

Returning to the flip-flop of Fig. 7, let us consider a typical set of marginal checking curves. The curves of Figs. 8 through 14 represent plots of the circuits components as a function of mcv excursion. Bistable circuits are generally simple circuits-to-marginal check since they fail by refusing to count, or frequency divide, rather than by failure to meet other required characteristics such as a specified rise time or voltage level. The curves of Figs. 8–14 mark the division between the regions of normal counting and failure to count.

Fig. 8 shows the permissible variation of R_{g2} and R_{c2} as a function of the mcv. Essentially the same curve would result for R_{c1} and R_{g1} but with opposite slopes. (*i.e.*, replace the symbols R_{g2} with R_{c1}, and R_{c2} with R_{g1}, on Fig. 6). From this curve it may be seen that any one resistor may drift approximately +45 per cent or −30 per cent before failure occurs. It also appears that an increase in the value of R_{g2} would provide more nearly equal positive and negative tolerances. This is easily evaluated by increasing the resistor and retaking the data. A comparison of the curves thus taken indicates which is the better of the two as far as balance is concerned. For a complete evaluation, however, many other factors must be examined. For example, consider Fig. 12 which shows the relation between the mcv and the trigger amplitude necessary for reliable operation. The circuit specifications include a minimum trigger level, and a change of R_{g2} may adversely affect circuit sensitivity. This would be reflected by loss of margin by Fig. 12 when R_{g2} is changed. Thus to evaluate completely a circuit change many related phenomena must be examined. This represents an extensive testing program which is sometimes economically justified only for circuits basic to the entire system.

Figs. 9, 10, and 11 are curves showing the relationship between the mcv and plate resistor, cathode resistor and tubes. Fig. 11 is generally difficult to obtain. Selected tubes are cometimes employed to simulate end-of-life characteristics. All too often these are "off-spec" by virtue of an internal mechanical deviation which introduces g_m or μ values significantly different from normal values and makes meaningful results impossible. Tubes with portions of the cathode material stripped have been used successfully, and the insertion of resistors in series with various electrodes has also been proven successful. These schemes must be employed judiciously,

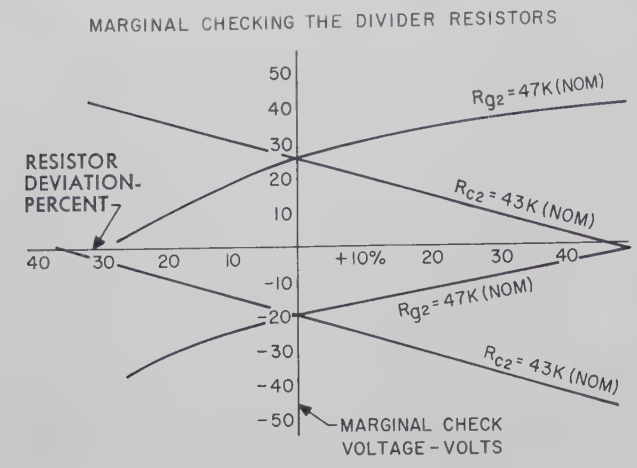


Fig. 8—Effect on marginal check voltage of deteriorating divider resistors (R_{g2} and R_{c2}) varied one at a time.

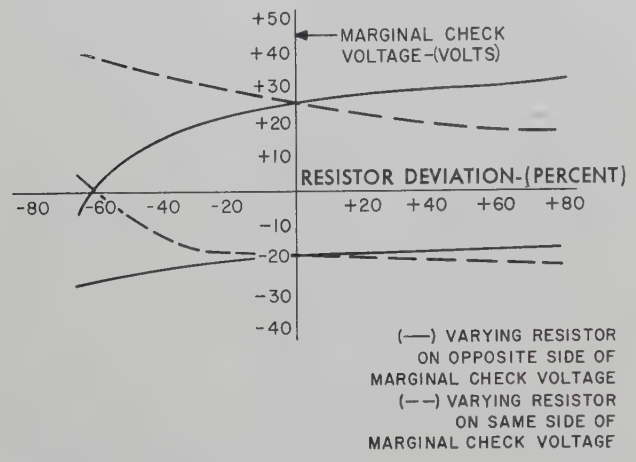


Fig. 9—Effect on marginal check voltage of deteriorating plate resistor.

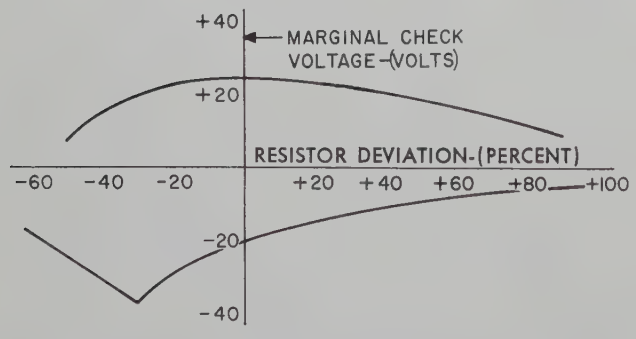


Fig. 10—Effect on marginal check voltage of deteriorating cathode resistor.

however, with the true effect on the circuit under test carefully examined. The data of Fig. 11 were taken by very carefully controlling the filament voltage to result in various values of i_b at fixed e_b. The tube was switched between the meter circuit and flip-flop circuit without interrupting filament current, and each test value of i_p

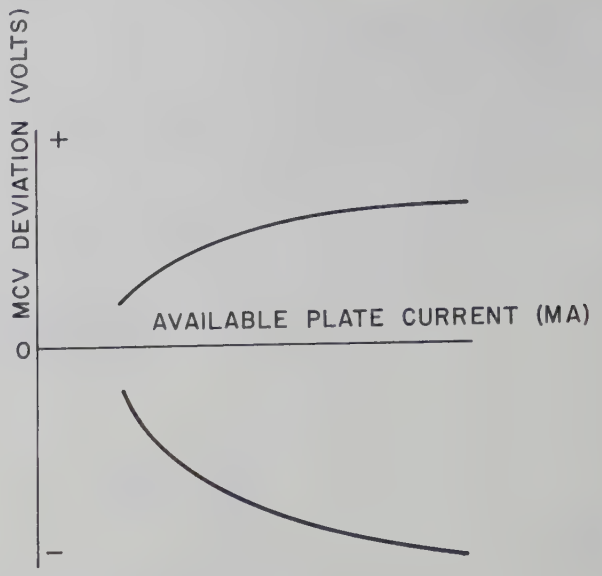


Fig. 11—Effect on marginal check voltage of simulated tube deterioration.

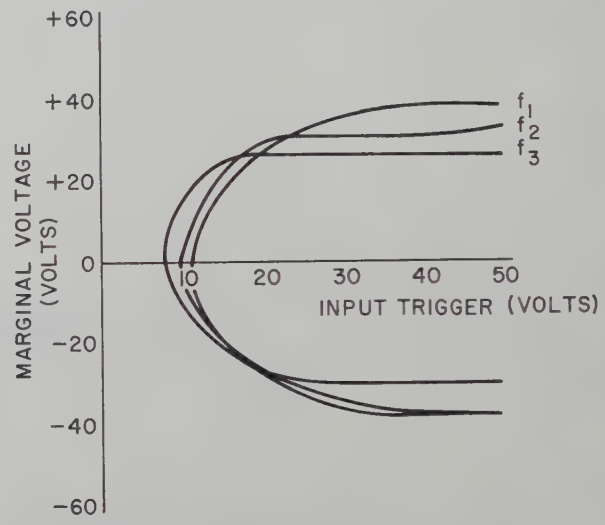


Fig. 12—Effect of trigger amplitude on marginal check voltage.

was checked immediately before and after each reading. If elaborate precautions are not taken, the data may not be repeatable.

Figs. 13 and 14 indicate an important use of marginal checking data. The exact load a circuit may drive is frequently an arbitrary or rule-of-thumb decision. Curves similar to Figs. 13 and 14 make the choice a quantitative one. With the peripheral conditions (*i.e.*, input amplitude, rep. rate, etc.) adjusted to the most severe extremes expected during normal operations, the load that can be driven for any specified loss of operating margin is quickly found. It is also possible to establish "initial" and "end-of-life" load conditions for determining complete output specifications.

A complete evaluation of flip-flop operation includes more than marginal check data. Curves of a type shown

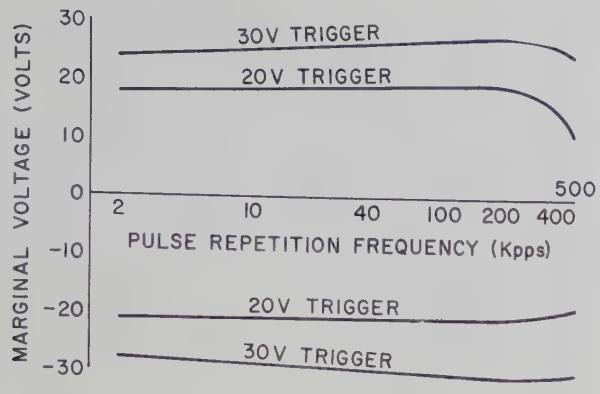


Fig. 13—Effect of trigger amplitude on the marginal check voltage at a function of frequency and driving equal loads on each plate.

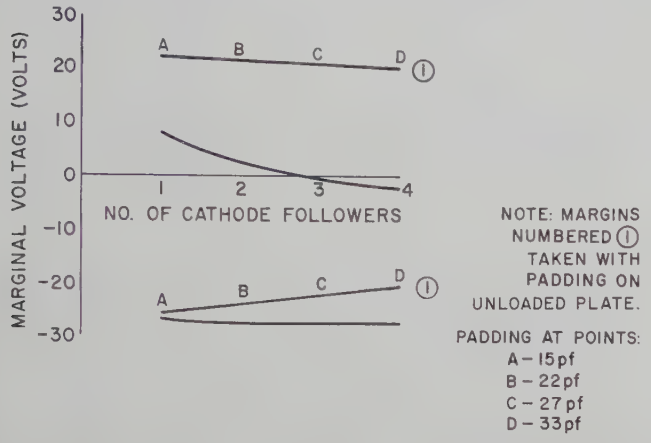


Fig. 14—Effect of equal and unequal plate loading on the marginal check voltage. Output plate drives cathode follower load. Unloaded flip-flop plate padded with capacity to ground.

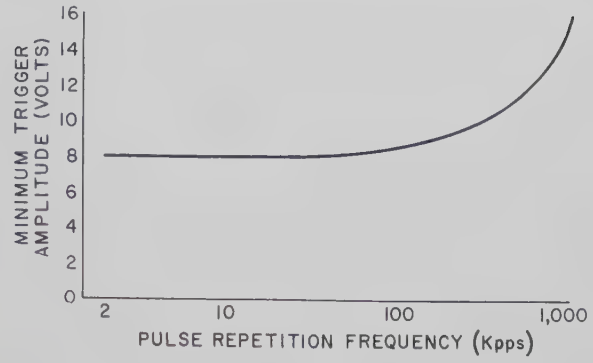


Fig. 15—Effect of prf on trigger amplitude.

by Fig. 15 (above) are necessary supplementary data.

One important aspect of marginal checking that flip-flop data do not illustrate is the need for a complete definition of circuit failure. Many circuits have very complex specifications establishing limits on current regulation, transition time, overshoot, and many other factors. For these circuits, at every point on the curve of component value vs mcv every factor must be considered; the first one violated establishes the permissible excursion of the mcv. Data of this type are invaluable not only to check the circuit design and insure that the mcv variations reflect the deterioration of all components, but also as an aid in the determination of the final excursion to be applied to the circuit when it becomes part of a system.

Reliability of an Air Defense Computing System: Marginal Checking and Maintenance Programming*

M. M. ASTRAHAN† AND L. R. WALTERS†

Summary—**Marginal checking by varying supply voltages for some time has been a means of preventive maintenance for electronic systems. Some important innovations have been employed in the marginal checking system of the AN/FSQ-7 air defense computer to give a more effective high-speed preventive maintenance technique. Completely automatic preventive maintenance testing is discussed incorporating program control of the marginal checking system.**

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HAVING DESIGNED and built a digital computer using the best available components and circuit techniques, one must still devise methods of maintenance, since even the best of components will deteriorate. The method of maintenance which has been devised for the AN/FSQ-7 Air Defense Computer involves the use of marginal checking and programming for the detection and location of imminent failures during periods of preventive maintenance.

Failure Prediction by Means of Marginal Checking

Marginal checking is used on a computer to detect components which have deteriorated to the extent that they might cause computer errors during ensuing operations. Marginal checking has been used by workers at M.I.T.[1–3] A computer voltage margin is defined as the amount of supply voltage excursion which will cause the computer to malfunction. This voltage margin is not quite the same as the circuit voltage margin which is defined in terms of standard input and output signals. There exists, however, a qualitative relation between circuit margins, as measured in bench testing, and computer margins. A large voltage margin is an indication that the computer will not malfunction during normal operation. A small voltage margin is an indication that a small change in some component value will cause computer malfunction. Assuming that components will change value gradually, rather than catastrophically, marginal checking properly employed, provides reasonable assurance that the computer will function reliably at least until the next scheduled maintenance period.

Circuits in a computer are not isolated; they exist in combinations with other circuits within large complex systems. The simplest approach to marginal checking in such a system would be to vary one of the power supplies serving the system, thus varying the corresponding voltage on all circuits at the same time. This method of power supply variation is popular in that it is the easiest to accomplish. It does produce some results and costs very little. This method of marginal checking has the following disadvantages:

1) Different circuits may require different excursions for the same effective prediction of failure. Use of a variable power supply for marginal checking puts the same excursion on all circuits which use that voltage, so that the circuits with small inherent margins may mask the failure prediction for those with large inherent margins.

2) It may be that the excursion required for effective prediction of one circuit may cause damage to another circuit, whether or not the other circuit is supposed to be marginally checked by that voltage.

3) The cascaded effects of voltage variation throughout the system may produce unrealistic indications of the computer's weakness.

To overcome these disadvantages, separate marginal checking lines with a series variable supply must be used. Use of a separate series variable supply enables the voltage to be varied on some circuits while others are receiving normal voltage.

In order to apply marginal checking voltages to selected groups of circuits, the power distribution system must be arranged so that each such group of circuits is supplied by a separate distribution line. Relays are employed to switch the variable supply in series with any selected line or group of lines, as shown in Fig. 1. Each individual line feeding a circuit or group of circuits is called a marginal checking line, and the assignment of these lines to given circuits or groups of circuits is called the marginal checking breakdown.

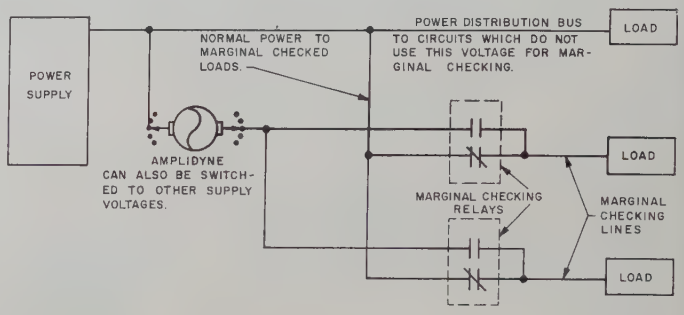

Fig. 1—The amplidyne provides a source of variable supply voltage. The marginal checking relays connect variable supply voltage to selected groups of circuits.

AN/FSQ-7 Marginal Checking System

The AN/FSQ-7 Computer is logically similar to M.I.T.'s Whirlwind and the IBM 701, but it is much larger and faster and has many special features to make it more efficient for its special application. The AN/FSQ-7 marginal checking system is a logical extension of the Whirlwind marginal checking system.

The marginal checking supply is an amplidyne, chosen because it is capable of supplying large currents and a well-regulated output voltage which can be precisely controlled over a wide positive to negative range. In particular, the voltage can be made precisely zero during switching, which greatly simplifies the switching problems. The amplidyne voltage, and therefore the magnitude of the excursion, is controlled by means of a potentiometer on the maintenance console. The marginal checking relays are controlled from the same location. They can be selected either individually or in groups. Thus the circuits on any line or group of lines can be marginally checked.

The Marginal Checking Breakdown

The organization of the marginal checking line selection is fundamentally important in understanding how the system is used and how the circuits are assigned to individual marginal checking lines. There are four major levels of selection. These are the marginal checking group, the voltage group, the circuit group, and the individual line as shown in Fig. 2.

[1] N. H. Taylor, "Marginal checking as an aid to computer reliability," Proc. IRE, vol. 38, pp. 1418–1421; December, 1950.

[2] N. L. Daggett and E. S. Rich, "Diagnostic programs and marginal checking in the Whirlwind I computer," 1953 IRE Convention Record, Part 7, pp. 48–54.

[3] R. J. Pfaff, "Marginal Checking for Circuit Designers," Div. 6 Memo. M-2459, Lincoln Lab., Mass. Inst. Tech., Cambridge, Mass.; October 13, 1953.

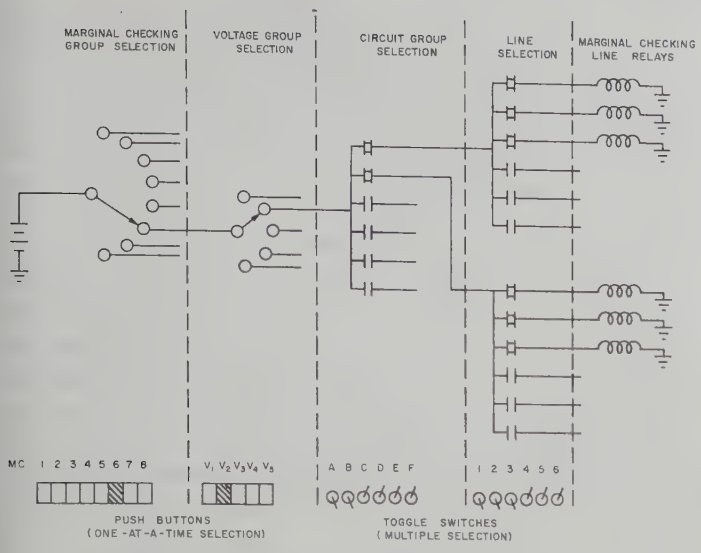

Fig. 2—A rapid go-no-go marginal check may be performed by transferring groups of marginal checking relays. If a failure is detected it can be localized by selecting marginal checking relays individually.

Marginal Checking Groups

The marginal checking lines are grouped into eight marginal checking groups. The marginal checking group is the largest section of the machine that can be marginally checked at one time. The limitation reduces the size of the amplidyne required. This limitation is not troublesome because the marginal checking groups correspond to major logical divisions of the equipment, such as Memory, Arithmetic Registers, Inputs, etc.

Voltage Groups

Within a marginal checking group there are five voltage groups. These groups correspond to the five specific supply voltages which have been chosen for marginal checking. Because there is only one amplidyne, only one voltage can be marginally checked at a time. Thus all the marginal checking lines for one voltage group in one marginal checking group represent the maximum number of lines to which an excursion can be applied simultaneously.

Circuits Groups

It is desirable to apply different excursions to different circuits even though they are marginally checked by means of the same supply voltage. This consideration leads to the third level of marginal checking selection called the circuit group. Within a voltage group those circuits which can be effectively marginally checked by approximately the same excursion are combined into circuit groups. There may be as few as one circuit group in a voltage group. The maximum number in a voltage group is six, which may be selected individually or in combinations.

Individual Lines

On the lowest level, the selection control system allows up to six individual lines in any circuit group, which can be selected individually or in combinations. The system provides for the selection of 1440 possible lines, of which some 700 are used. These lines serve equipment containing over 16,000 tubes.

Prescribed Excursions as a Means of Imminent Failure Detection

The marginal checking system is used to detect those imminent failures which are indicated by decreasing margins. An obvious way to employ such a system is to periodically examine the margins for significant decay. This would be accomplished by applying a voltage excursion which is gradually increased until failure occurs. The magnitude of the excursion at the instant of failure is the voltage margin for that line.

An alternate method, more practical to employ, is to establish prescribed or fixed excursions such that if the existing margins are greater than these excursions, the machine can be expected to operate without error for an extended period of time. This testing method requires only the application of the prescribed excursions to the marginal checking lines and a test for malfunctions. If no malfunctions occur, the margins are greater than the prescribed excursions. Testing with fixed excursions offers the following advantages over the routine measurement of margins:

1) It is easier to apply a fixed excursion and test for malfunctions, than to apply an ever-increasing excursion until malfunction occurs.

2) Routine measurement of margins would result in large volumes of data, all of which would have to be analyzed and compared with previous data to determine when a component should be replaced. With fixed excursions, only malfunctions need be investigated.

The prescribed excursion must be large enough to simulate the effect of normal variations of environment, such as temperature, supply voltage, regulation, and noise. In addition, the prescribed excursion must be large enough to simulate the effect of maximum component deterioration, which may occur before the next marginal checking period. On the other hand, setting the prescribed excursion too high will result in premature replacements of components. The costs of premature replacements of components are increased maintenance time and increased risk of failure because of new components.

Fig. 3 indicates a hypothetical curve of the probability of a given circuit causing computer failure within a given time vs that circuit's margin. It is expected that the curve will have a knee such that if the circuit margin is greater than a certain value of X volts, the probability of that circuit causing computer failure within Y days is

extremely low. The prescribed excursion would be set at or slightly above X volts if Y represents the maximum number of days that can elapse before the next marginal checking period.

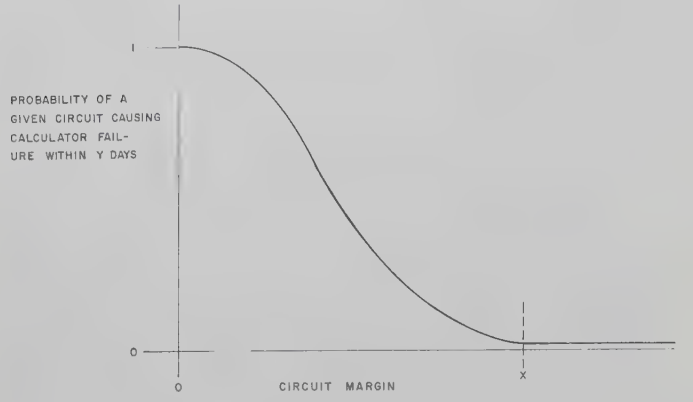

Fig. 3—The probability of circuit approaches unity as the margin approaches zero. If the margin is higher than "x" volts, the probability of failure is very low. This value "x" is determined and used for a go-no-go reliability check.

Use of Programming in the Detection of Imminent Failures

To detect an imminent failure, all machine operations must be exercised, checking the results of each operation for error. These operations may be exercised by means of programs, or by special test equipment which will generate input signals and measure or test output signals. Making maximum possible use of programs for error detection has the following advantages over the use of special test equipment:

1) The program can easily be changed whenever the machine, or part of the machine is changed, and in addition, the program can be constantly improved.

2) The program requires no extra equipment, it uses the computing facilities which are already available.

3) The program uses the machine in a more normal manner than test equipment could use it.

4) A checked out program is not subject to deterioration as is test equipment.

Nonmarginal Checking Reliability Programs

The computer maintenance programs which are used to detect the existence of errors with or without excursions are called reliability programs. Reliability programs are used without marginal checking excursions to detect existing failures and with marginal checking excursions to detect imminent failure.

Before applying excursions the computer must operate without error with voltages normal. This is accomplished by running reliability programs designed specifically for this purpose. The programs for testing the computer with no excursions applied are called nonmarginal checking reliability programs. These programs are written under the assumption that anything might be wrong with the computer; therefore they must be written to minimize the possibility of any errors giving a false indication of successful operation. These programs are based on a hierarchy of testing wherein certain basic operations are first tested exhaustively, and then the remaining, more complex operations can be tested using these basic operations as tested tools.

Marginal Checking Reliability Programs

When it has been determined that the machine runs correctly with no excursions applied, it can be assumed during marginal checking that only those portions of the machine to which excursions are applied will malfunction. Thus, the marginal checking reliability programs can be written to test very thoroughly each portion of the machine in turn using all other portions without the risk of having confusing multiple failures and malfunctions.

The Use of Marginal Checking and Programming in the Location of Imminent Failures

When the existence of an imminent failure has been detected by marginal checking and reliability programs, it is necessary to locate the component which caused the malfunction. Localization of the deteriorated component is facilitated by means of the marginal checking breakdown and diagnostic programming. Since the computer operated correctly with no excursion applied, it can be assumed that the malfunction must be in the circuits to which the excursion was applied, or in circuits adjacent to them. Adjacent circuits are those containing series signal paths without intermediate regeneration of the signal. Flip-flops and level setters are examples of circuits which regenerate the signals. Cathode followers and pulse amplifiers are examples of circuits which do not regenerate signals completely. The marginal checking breakdown provides a means of marginally checking selected circuits.

The first three levels of the marginal checking breakdown, namely, marginal checking group, voltage group, and circuit group, are inherent to the system for imminent failure detection. The circuit group contains several lines which can be separately marginally checked for imminent failure location. Subdivision of the circuit group is provided based on logical function. Clearly the fewer circuits there are per marginal checking line, the easier the task of locating the component causing the malfunction. However, the number of marginal checking lines is limited both by cost and by the effect upon system reliability. Each marginal checking line requires a relay in the power distribution system, appropriate circuit breakers, and control relays. These components contribute to cost and detract from system reliability. Thus a compromise must be reached between ease of imminent failure isolation and these cost considerations.

The program which was used to detect an imminent failure can be used in conjunction with the logical breakdown to isolate it to those circuits on a single marginal

checking line. Further localization of the imminent failure must be accomplished by diagnostic programs and procedures. The art of diagnostic programming will not be treated here, but two basic principles of diagnostic programming will be given as examples. The first principle deals with the parallel processing of data. When information is processed in parallel it is usually possible to test all channels simultaneously and to determine from the result which channel, if any, has failed. The second principle deals with the optional selection of equipment. A program can easily isolate a failure to the smallest element which it can exercise separately. However, control circuitry, which is not employed by every instruction, must be diagnosed for failures by a hierarchy of tests which first verify basic control circuitry with simple programs before proceeding to the more complex programs to be used for verifying the remaining control circuitry.

In making a marginal checking breakdown, diagnostic programming should be considered. For example, separate marginal checking lines could be provided for elements which cannot be separately exercised by a program. However, there would be no point in providing separate lines for each position of a register, for example.

Automatic Marginal Checking

Since the maintenance procedure of running programs and applying excursions to the computer is routine, the computer can supervise it. To make the procedure completely automatic all that is needed is to provide means for the computer to control the marginal checking system.

The AN/FSQ-7 computer is able to direct information to the marginal checking system, specifying the selection of the marginal checking lines, the magnitude and polarity of the excursion to be applied, and the time duration of the excursion. A control program can then initiate the marginal checking excursion. The test program is started after the excursion reaches its steady state and the excursion is terminated either on the conclusion of the test program or after a preset time interval determined by a mechanical timing device. The control program is automatically restarted when the excursion has been removed. The results of the test can be printed and a new test started.

This completely automatic operation has the advantages of speed and accuracy. Both the test program and the marginal checking control data are stored in punched cards or on magnetic tape. To carry out the complete test procedure, the operator need only load the cards or tape, press the start button, and examine the results from the printer. The high-speed computer need not idle while the maintenance engineer manually operates the controls. The testing process is not subject to the human errors that accompany routine tasks. The equipment cost of this automatic control of marginal checking is justified where maintenance time must be held to a minimum.

Correspondence

The Detection and Identification of Symmetric Switching Functions with the Use of Tables of Combinations*

Introduction

As noted by Shannon,[1,2] symmetric switching functions lead to relay contact networks which are much more economical of elements than the best series-parallel circuit. Shannon defines a symmetric function as follows: "A function of the n variables $X_1, X_2, \cdots, X_n$ is said to be symmetric in these variables if any interchange of the variables leaves the function identically the same. Thus $XY+XZ+YZ$ is symmetric in the variables X, Y, and Z. Since any permutation of variables may be obtained by successive interchanges of two variables, a necessary and sufficient condition that a function be symmetric is that any interchange of two variables leaves the function unaltered. By proper selection of the variables many apparently unsymmetric functions may be made symmetric. For example, $XY'Z+X'YZ+X'Y'Z'$ although not symmetric in X, Y, and Z is symmetric in X, Y, and Z'."

Possibly because of the difficulty in detecting and identifying this latter type of symmetric function, treatment of it has been omitted from almost all of the subsequent work in this field. For example, Washburn[3] writes: "A symmetric relay-contact network is one in which the conditions for closing a particular input-to-output path are given . . . in terms of the number of relays operated and unoperated. For example, a network which is closed when any three . . . out of five relays are operated is a symmetric circuit." Similarly,[4] a symmetric network is exemplified as one which is closed when "m out of n" relays are operated. The "m out of n" type of network is related to symmetric functions having variables of symmetry which are either all unprimed or all primed. All other symmetric functions have some but not all of the variables of symmetry primed. Since there are 2^n ways of priming n variables of symmetry, and only two of these result in the variables being either all unprimed or all primed, there are 2^n-2 ways which are not associated with the "m out of n" type of circuit. Therefore, it can be seen that the "m out of n" networks account for only a small portion of the symmetric functions as defined by Shannon.

The recognition of symmetric functions other than the all unprimed or all primed type is very difficult by algebraic means.

* Received by the PGEC, June 13, 1956.

[1] C. E. Shannon, "A symbolic analysis of relay and switching circuits," *AIEE Trans.*, vol. 57, pp. 713–723; 1938.

[2] C. E. Shannon, "The synthesis of two-terminal switching circuits," *Bell Sys. Tech. J.*, vol. 28, pp. 59–98; 1949.

[3] S. H. Washburn, "Relay trees and symmetric circuits," *AIEE Trans.*, vol. 68, pp. 582–586; 1949.

[4] W. Keister, A. E. Ritchie, and S. H. Washburn, "The Design of Switching Circuits," D. Van Nostrand Company, Inc., New York, N. Y., article 4.10; 1951.

All combinations of primed and unprimed variables could be investigated and tested for symmetry, but with a large number of variables such a method would be manually impractical. Caldwell[5] has described a method of recognizing and identifying symmetric functions with the use of a map (chart) similar to those developed by Veitch[6] and Karnaugh.[7] As Caldwell points out, however: "When the number of variables of symmetry exceeds four, the direct recognition of symmetric functions by chart patterns becomes quite difficult." When more than four variables are involved, therefore, the procedure is complicated by the necessity of using a multiplicity of maps and an expansion theorem for symmetric functions.

Two essentially prime-counting methods of detecting and identifying general symmetric switching functions, with the use of a table of combinations, are presented here. These methods are simple and quickly accomplished, regardless of the number of variables involved. A general method leads to a determination of symmetry or lack of symmetry under all possible conditions. A contingent method has the advantages of being slightly simpler than the general method and in the majority of cases of being faster to perform. However, in one case it will not yield a solution, and the general method will have to be employed.

Preparation of Table for Both Methods

The switching function to be examined is written as a table of combinations (truth table). Here a "1" is used to denote truth and a "0" is used to denote falsity, although the choice is purely arbitrary. At the head of each column the denoted variable is written unprimed.

Example:

function:	$XY'Z+X'YZ+X'Y'Z'$[8]		
table:	X	Y	Z
	1	0	1
	0	1	1
	0	0	0

The table should be checked to assure that no row combination occurs more than once.

General Method (See Fig. 1)

The arithmetic sum of each row in the table is obtained and written to the right of the row. All row sums are checked for sufficient occurrence: if n represents the number of variables (columns), and r represents a row sum, then that row sum should occur $n!/r!(n-r)!$ times. (Table I above.[9]) (This is the formula for the number of combinations of n things taken r at a time.)

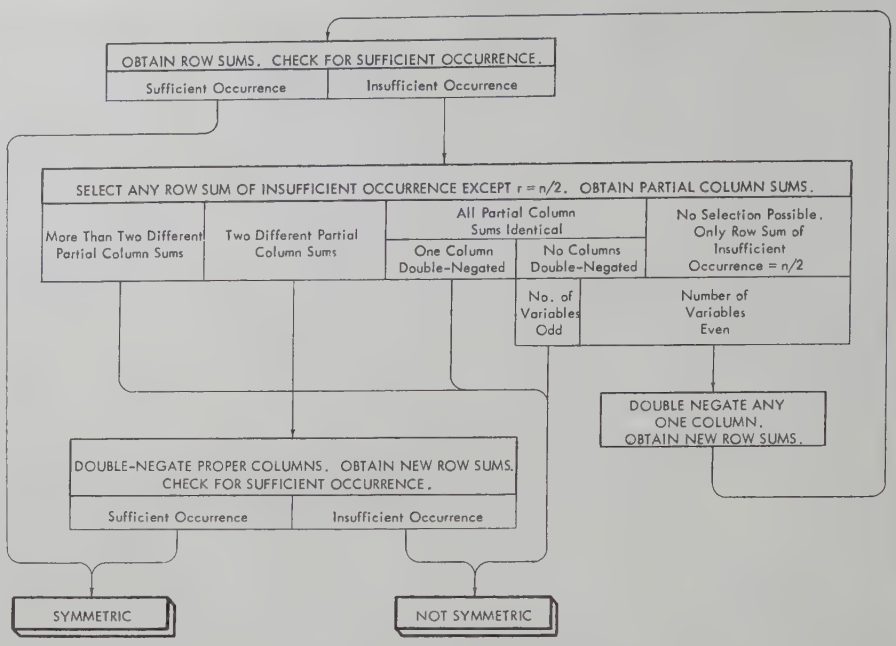

Fig. 1—General method—block diagram.

TABLE I
Table of Required Row Sum Occurrence

Row Sum	Required Occurrence of Row Sum: Number of Variables							
	1	2	3	4	5	6	7	8
0	1	1	1	1	1	1	1	1
1	1	2	3	4	5	6	7	8
2		1	3	6	10	15	21	28
3			1	4	10	20	35	56
4				1	5	15	35	70
5					1	6	21	56
6						1	7	28
7							1	8
8								1

If all row sums occur the required number of times, the function is symmetric. The row sums are the a-numbers,[10] and the variables of symmetry are denoted at the head of the columns.

Example:

X	Y	Z	
1	0	0	1
0	0	1	1
0	1	0	1

n (number of variables) = 3
r (row sum) = 1.

Required occurrence of

$$1 = \frac{n!}{r!(n-r)!} = \frac{3!}{1!2!} = 3.$$

The row sum (1) occurs the required number of times (3); therefore the function is symmetric and can be expressed as $S_1(X, Y, Z)$.

Example:

X	Y	Z	
1	1	0	2
1	1	1	3
1	0	1	2
0	1	1	2

$n = 3$

$r_1 = 2.$

Required occurrence of

$$2 = \frac{3!}{2!1!} = 3$$

$n = 3$

$r_2 = 3.$

Required occurrence of

$$3 = \frac{3!}{3!0!} = 1.$$

Both row sums (2 and 3) occur the required number of times (3 and 1 respectively); therefore the function is symmetric and can be expressed as $S_{2,3}(X, Y, Z)$.

If any row sum does not occur the required number of times, any one row sum of insufficient occurrence *except* $r=n/2$[11] is selected, and only the rows totaling this sum are considered in obtaining a partial arithmetic sum of each column.

[5] S. H. Caldwell, "The Recognition and Identification of Symmetric Switching Functions," AIEE Tech. Paper 54-24, 1954.

[6] E. W. Veitch, "A chart method for simplifying truth functions," *Proc. of the Assn. for Comp. Machinery*; May, 1952.

[7] M. Karnaugh, "The Map Method for Synthesis of Combinational Logic Circuits," *AIEE* Tech. Paper 53-217, 1953.

[8] The transmission concept is used in this paper. The hindrance concept is used by Shannon, *loc. cit.*; the distinction should carefully be noted in footnote 10.

[9] Table I is a table of required row sum occurrence for a maximum of eight variables. This table is an adaption of Pascal's Triangle and may be extended to include as many variables as desired.

[10] The following theorem is from Shannon, *loc. cit.*, "A necessary and sufficient condition that a function be symmetric is that it may be specified by stating a set of numbers $a_1, a_2, \cdots, a_k$ such that if exactly $a_j (j=1, 2, 3, \cdots, k)$ of the variables are zero, then the function is zero and not otherwise. This follows easily from the definition. The set of numbers $a_1, a_2, \cdots, a_k$ may be any set of numbers selected from the numbers 0 to n, inclusive, where n is the number of variables in the symmetric function. For convenience, they will be called the a-numbers of the function. The symmetric function $XY+XZ+YZ$ has the a-numbers 2 and 3, since the function is zero if just two of the variables are zero or if three are zero, but not if none or if one is zero. To find the a-numbers of a given symmetric function it is merely necessary to evaluate the function with 0, 1, $\cdots$, n of the variables zero. Those numbers for which the result is zero are the a-numbers of the function."

The symmetric function illustrated in the theorem may be expressed symbolically as $S_{2,3}(X, Y, Z)$. [It may also be expressed as $S_{0,1}(X', Y', Z')$ since any symmetric function of n variables is equal to the symmetric function of the corresponding negated variables when each a-number a_j of the original function is replaced by the a-number $(n-a_j)$.] The function $XY'Z+X'YZ+X'Y'Z'$ has the a-number 1 with the variables of symmetry X, Y, Z'; therefore, it may be expressed as $S_1(X, Y, Z')$ [and also as $S_2(X', Y', Z)$].

[11] A row sum equal to one-half the number of variables can occur, of course, only if the number of variables is even.

1) If more than two different partial columns sums occur, the function is not symmetric.
2) If two and only two different partial column sums occur, either one of these sums is selected (preferably the one of lesser occurrence) and all columns (in the original table) which contain this partial sum are double-negated: all 1's are changed to 0's, all 0's are changed to 1's, and the variables at the head of these columns are primed. New row sums are obtained and checked for sufficient occurrence.

Example:

X	Y	Z	
1	0	1	2
0	1	1	2
0	0	0	0
1	1	1	3
1	0	0	1
0	1	0	1

≡

X	Y	Z'	
1	0	0	1
0	1	0	1
0	0	1	1
1	1	0	2
1	0	1	2
0	1	1	2

X	Y	Z	
1	0	1	2
0	1	1	2
1	1	2	

Conditions for symmetry are as in the first step; if any row sum does not occur the required number of times, the function is not symmetric.

3) If the number of variables is odd and all partial column sums are identical, the function is not symmetric. If the number of variables is even and all partial column sums are identical, or if the only row sum of insufficient occurrence is equal to one-half the number of variables so that no row sum selection may be made, any one column is selected at random and double-negated, and new row sums are obtained. The method is repeated once; if, on this repetition, all partial column sums are identical, the function is not symmetric.

Contingent Method (See Fig. 2)

The arithmetic sum of each column in the table is obtained and written at the foot of the column. If more than two different column sums occur, the function is not symmetric. If two and only two different column sums occur, the total of these two sums is obtained and compared with the number of rows in the table.

1) If the total of the two different column sums is not equal to the number of rows in the table, the function is not symmetric.
2) If the total of the two different column sums is equal to the number of rows in the table, either one of these sums is selected (preferably the one of lesser occurrence), and all columns totaling the selected sum are double-negated. (If the selected column sums are corrected to represent the new total for the double-negated columns, all column sums will now be found to be identical.) The row sums are obtained and checked for sufficient occurrence.

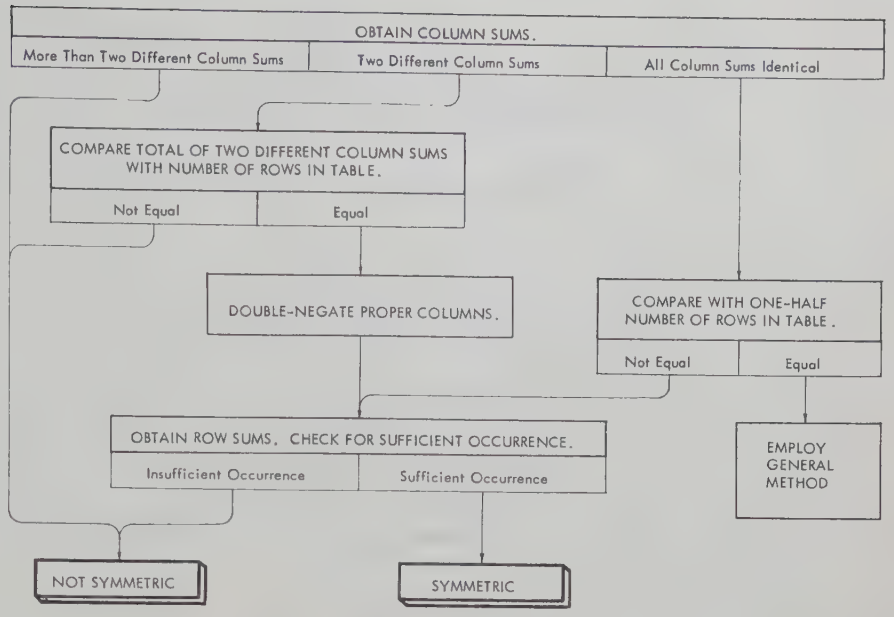

Fig. 2—Contingent methods—block diagram.

Example:

X	Y	Z	
1	0	1	
0	1	1	
0	0	0	
0	0	1	
1	1	3	

≡

X	Y	Z'	
1	0	0	1
0	1	0	1
0	0	1	1
0	0	0	0
1	1	1	

$1 + 3 = 4$ = the number of rows in table.

A	B	C	D	E
0	1	1	1	1
1	1	1	0	1
1	1	1	1	0
1	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	0
0	0	0	0	0
5	6	6	5	5

≡

A	B'	C'	D	E	
0	0	0	1	1	2
1	0	0	0	1	2
1	0	0	1	0	2
1	1	1	1	1	5
0	1	0	0	1	2
0	1	0	1	0	2 ≡ $S_{2,5}(A,B',C',D,E)$
0	0	1	0	1	2
0	0	1	1	0	2
1	1	0	0	0	2
1	0	1	0	0	2
0	1	1	0	0	2
5	5	5	5	5	

Conditions for symmetry are as in the first step of the general method. If any row sum does not occur the required number of times, the function is not symmetric.

If all column sums are identical, they are compared with one-half the number of rows in the table.

1) If the column sums are not equal to one-half the number of rows in the table, the row sums are obtained and checked for sufficient occurrence. Conditions for symmetry are as in the first step of the general method. If any row sum does not occur the required number of times, the function is not symmetric.
2) If the column sums are equal to one-half the number of rows in the table, the general method must be employed.

Supplement

Illustration

Following is an illustration of the table method applied to the function:

$$A'BCDE+ABCD'E+ABCDE'+AB'C'DE+A'B'CD'E+A'B'CDE'+A'BC'D'E+A'BC'DE'+AB'CD'E'+ABC'D'E'+A'B'C'D'E'$$ [5].

The contingent method is used.

Conditions for symmetry are as in the first step of the general method. If any row sum does not occur the required number of times, the function is not symmetric.

If all column sums are identical, they are compared with one-half the number of rows in the table.

1) If the column sums are not equal to one-half the number of rows in the table, the row sums are obtained and checked for sufficient occurrence. Conditions for symmetry are as in the first step of the general method. If any row sum does not occur the required number of times, the function is not symmetric.
2) If the column sums are equal to one-half the number of rows in the table, the general method must be employed.

Contact Network

Once the symmetric function has been detected and identified, it is a simple matter to design the actual relay contact network.[1,3,4] As an example, the relay contact network for the function $S_3(A, B', C, D, E')$ is shown in Fig. 3.

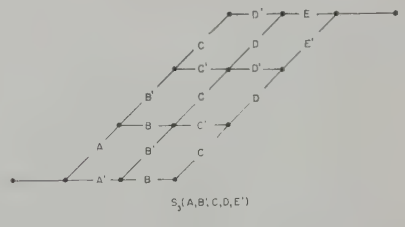

Fig. 3

Mitchell P. Marcus
Internatl. Business Machines Corp.
Endicott, N. Y.

Symposium
The Design of Machines to Simulate the Behavior of the Human Brain*

At the 1955 IRE National Convention the PGEC sponsored a symposium, "The Design of Machines to Simulate the Behavior of the Human Brain." The four panel members were Warren S. McCulloch of M.I.T., Anthony G. Oettinger of Harvard, Otto H. Schmitt of the University of Minnesota, and Nathaniel Rochester of IBM. The moderator was Howard E. Tompkins, then of Burroughs Corporation.

After the panel members' prepared statements, and a brief discussion, a group of invited questioners cross-examined the panel members. The invited questioners were: M. L. Minsky of Harvard University, Morris Rubinoff of the University of Pennsylvania, Elliot L. Gruenberg of the W. L. Maxson Corporation, John Mauchly of what was then Remington Rand, Inc., M. E. Maron, then of IBM Corporation, and Walter Pitts of M.I.T. Finally, Jerome Rothstein of the Signal Corps Engineering Laboratories contributed some observations from the floor.

The original transcript of the Symposium has been edited by the speakers with the help of Mr. Tompkins, chairman of the Symposium.

"Brain," A Computer With Negative Feedback

W. S. McCULLOCH: Since nature has given us the working model, we need not ask, theoretically, whether machines can be built to do what brains can do with information. But it will be a long time before we can match this three-pint, three-pound, twenty-five-watt computer, with its memory storing 10^{13} or 10^{15} bits with a mean half-life of half a day and successful regeneration of 5 per cent of its traces for sixty years, operating continuously with its 10^{10} dynamically stable and unreplaceable relays to preserve itself by governing its own activity and stabilizing the state of the whole body and its relation to its world by reflexive and appetitive negative feedback.

Its general organization was first guessed from the disorders of its circuit action, produced by destruction of its parts. The body's transducers, called sense organs, excited by light, sound, taste, smell, touch, temperature, pressure, length, acceleration, and so on, send signals to the back of the nervous system. The expansion of the back of the top of the nervous system is called the brain. Its front sends signals to muscles and glands to stop, reverse, or modify the process reported by the sense organs.

Highest in the brain is the cerebrum with its bark, or cortex, some hundred relays deep, connected in both directions on its input side with large banks of relays called the thalamus. Without these structures, we cannot see shapes or hear tunes or compute any of the other invariants we call perceptions, or ideas. Wedged between the bark and thalamus are the basal ganglia, which program our automatically associated movements, like sucking, eating, crawling, walking, running, and so on. The bulge at the back of the brain is called the cerebellum. Its business is to bring to rest at the proper place whatever part of the body has been put in motion.

Each of these parts of the brain sends signals to others, and all of them send signals over many channels to many parts of the nervous system where they play on the output side of the servosystem which we call reflex arcs. The storage of traces, our memory, is of many kinds and cannot be simply located. Most of it cannot lie in the cerebellum or below it. So much for the general scheme.

Now for the components. These are living cells—neurons. A typical one has branches about one millimeter long, a body about ten thousandths of a millimeter across and a long thin taproot which may be anything from a millimeter to a meter long. The taproot ends in fine branches on other neurons, or goes out to glands or muscles.

Anatomy of the nervous system discloses the arrangement of these neurons, that is, the wiring diagram of the subassemblies of our computers. For example, consider the bark of the cerebellum (the organ which brings to rest anything which is put in motion). It is much the same everywhere. Inputs from the pickups in the body come to small relays on the bottom and go up into the cerebellum by fine T-shaped taproots. The rest of the brain plays on it through other entering leads, and its output is through its largest cells. So much for a typical wiring diagram.

Now for the signals, which we follow electrically. Every neuron burns sugar and oxygen to get the energy to keep its skin about a tenth of a volt positive outside. The skin is so thin that its capacitance is one microfarad per square centimeter. The resistance of the skin is extremely nonlinear, being high for all voltages above about a third of that resting voltage and vanishing for smaller values. So whenever the outside is driven that far negatively, the skin shorts locally, drawing current from the adjacent outside and sending it along the inside which has a conductance about like that of dilute salt water. This discharges the neighboring membrane which in turn shorts locally, and so the impulse is propagated

* Manuscript received by the PGEC, July 9, 1956.

along this distributed repeater. The velocity of propagation clearly depends upon the distributed resistance, the distributed capacitance, and the distributed supply of energy.

As you might guess from the dimensions and from the Kelvin equation, the velocity ranges from about 150 meters per second in fat taproots to less than one meter per second in fine ones.

The factor of safety for propagation of the signal in a fiber of uniform diameter is about ten to one, but the mismatch at branch points, where the signal hits the fine fibers, brings the safety factor down to about one. This is important because at these places the number of impulses that get through will depend upon the local state of the fiber, and so upon any stray currents in the ground in which all neurons are embedded.

Since a nervous impulse appears to this ground as a sink of current, preceded and followed by a source of current, the impulses in neighboring fibers near the fine branch points will facilitate or block conduction in them, according to their time relationships. This is one way of gating signals by signals and we know that it is one used by the nervous system.

The second way is somewhat similar, for stray currents may also alter the threshold of the neuron next in line and so alter the number, size, and arrangement of impulses required to fire it. We have good reason to believe that the brain uses this trick also. The impulse and partial recovery take about one millisecond, but sustained frequencies above 250 per second have rarely been recorded. The precision of time of initiation of an impulse and of the fall-off of addition of signals which are not quite simultaneous is of the order of 30 microseconds. This means that pulse-interval modulation is more efficient than simple all-or-none binary coding and there is increasing experimental evidence that much information from our transducers is so coded.

One thing is not so coded: position of transducers in the body. This is coded into which fiber is firing and so into position in the brain. Actually, neighborhood is again and again represented by neighborhood even where there are multiple mappings on the bark of the cerebrum and on the bark of the cerebellum. Thus topological properties are automatically preserved. This, as opposed to the use of position to represent powers of a radix, gives brains, despite their digital tricks, the chief advantage of analog devices in which an error is usually in the last place.

Neighborhood-to-neighborhood projection over many imperfect channels in parallel insures performance which is surprisingly little perturbed by perturbation of signals, of thresholds, and even of the details of their connections. This fact is important because scattered, irreplaceable neurons are always dying, and because the information in our genes could prescribe no more than statistical regularities in the connection of neurons. The specifications for the body and brain are all initially coded in amino acids about as numerous as the letters of the alphabet, strung out on our chromosomes, and could all be printed without redundancy in the one hundred pages of your abstracts, something on the order of 10^7 bits. It is up to the geneticist to crack the code, while we, the neurophysiologists, have to work out the circuit action.

Contrasts and Similarities

Anthony G. Oettinger: Many suggestive analogies have been proposed between certain functions and components of digital computers on the one hand, and functions and components of animal nervous systems on the other. These have attracted considerable attention to the problem of simulating the behavior of the human brain by means of inanimate mechanisms. The problem of simulation arises in two types of research activities which, although related, are far from being identical. The first is the study of animal nervous systems, the second is the development of machines themselves.

In normal operation, the automatically-sequenced digital computer indeed performs many functions heretofore associated only with the human brain. Furthermore, it can readily be programmed to simulate many functions for which it was not specifically designed. Machines have been built or programmed to play games, and to simulate conditioned reflexes and such higher modes of behavior as maze-solving and pattern recognition. Computers might therefore be very useful in the study of animal nervous systems, as tools for testing and evaluating theoretical models of brain structure and functions. In practice this may be accomplished in two distinct fashions.

First, if a given theory is formulated in mathematical form, the computer can be used exactly as for ordinary engineering problems, to obtain numerical values of pertinent functions, to solve differential equations, and so forth. The Harvard Mark IV Calculator has recently been used in this fashion by Mosteller and Bush, in connection with a theory of learning.

On the other hand, a theory may assert that a set of model neurons interconnected in a particular fashion should react in a specific manner under given environmental conditions. In this case, the digital computer may be programmed to simulate the neuron network together with its environment. Experiments may then be performed to ascertain whether or not the model neuron network indeed performs as expected. Mr. Rochester will, I believe, describe some experiments of this type.

It may therefore be expected that computers will come to play as significant a role in neurophysiological and psychological investigations as they already have in engineering applications.

Now, with regard to the second problem, that of the development of machines, one may ask to what degree knowledge of the brain can be of service to the machine designer. Present computers are superior to the human brain in the performance of a number of functions. Their speed and accuracy in performing arithmetic operations, for example, are vastly superior to those of

the best calculating prodigies. But, as regards freedom from gross failures, and especially as regards adaptability to new situations, no present machine can match the human organism.

A digital computer is indeed flexible, in that it can solve a large variety of problems. But each problem is solved according to a different program supplied to the machine by human intervention. The human being, on the other hand, is provided at birth with the means for successful adaptation to situations of a variety totally out of the reach of any present machine.

Thus, if our goal is the design of more reliable, more adaptable machines capable of uninterrupted operation over periods of many decades, then living organisms provide, so to speak, an existence theorem guaranteeing the reality of this goal. But, like so many existence theorems, this one in no way specifies how the goal may be attained. Granted, then, that the simulation of certain higher mental functions is a goal of considerable theoretical and practical importance, it remains to find ways of reaching this goal.

The first thought, most naturally, is to imitate the functions of living organisms by also imitating what is known or hypothesized about their structure. A growing number of workers are channeling their efforts in this direction. One hopes that these efforts will be successful, since their success is likely to be of importance to both neurophysiology and machine design.

However, while attempts to imitate the structure of living organisms are of great potential value, it should not be overlooked that many of the most successful simulations of living functions and, indeed, superior performances of these functions, have often been achieved by means not generally used by living organisms.

For example, while the flight of birds undoubtedly stimulated man's urge to fly, human flight was achieved by significantly different means. At least one of our best mechanical tools, the wheel, has no counterpart in animal organisms. Arithmetic operations are performed in digital computers using algorithms significantly different from those congenial to the conscious human brain.

The structure of the apparatus which performs these operations differs from machine to machine, and has no necessary correspondence with the structure of the elements of the brain performing similar functions. It can be expected, therefore, that many machines of the future will continue to have only a functional resemblance to living organisms.

It is not possible to state how one might design machines functionally identical with living organisms, whether structurally identical or not, since such machines do not exist as yet. Something can be said, however, about the problem of reliability. In particular, the following example indicates why, in a specific instance, the simulation of natural structures is not necessarily desirable.

It is a reasonable assumption that the probability of failure in the operation of a relay is of the order of 10^{-7}. If a decimal number is represented by four binary digits held in four relays, the probability of an error in this number is roughly 4×10^{-7}. The addition of a fifth relay to provide a parity check reduces the probability of an undetected error to the order of 10^{-13}, with an increase in equipment of only 25 per cent.

Now nature seems to operate in a different way, by multiplexing to a very large degree, because the elements it uses are generally less reliable than the relays. Starting with elements with a probability of failure of the order of 10^{-3}, von Neumann estimates that, as an upper bound of the order of 10^{4}, such elements must be used to reduce the probability of malfunction to a range equivalent to that obtained by the parity check digits, and this is on the assumption that the state of a specified majority of these elements defines the state of the set. Now, in the relatively sheltered conditions under which most of our computers operate, the use of parity checks seems unquestionably the more economical solution at present.

As for the future, while nature seems to have settled on the use of relatively fragile biochemical units as the building blocks of living systems, new computer components of greater intrinsic reliability are being developed. The stability and reliability of new magnetic devices has resulted in significant increases in computer reliability. The use of solid-state devices shows similar promise. It is conceivable, therefore, that desired levels of machine reliability may be attained more economically through the use of components of sufficiently high intrinsic reliability, rather than through the multiplication of components of relatively low intrinsic reliability.

Two paths thus seem open, both leading to an ever-closer simulation of the behavior of the human brain: one following the example of nature, the other following avenues she has not cared to explore. In attempting to follow the example of nature through the study and simulation of animal nervous systems, we can expect to learn more about her ways, and this increased knowledge may, in turn, benefit the computer art. But it can be expected that many computing and control problems will continue to be solved most easily and most economically by the use of structures unknown in living organisms, and that, to this extent, the paths of physiology and of machine design will continue to diverge.

Simulation of Brain Action on Computers

Nathaniel Rochester: The automatic calculator is a new tool which can be brought to bear on the problem of how the brain works just as it is being applied, for example, to the problem of transient heat flow in a jet engine. In the study of transient heat flow there is no attempt to draw analogies between the structure of the calculator and a jet engine. Instead, the calculator is set up so that it produces a set of numbers which are

supposed to correspond in some way to the flow of heat.

Fig. 1 shows a typical course of a research problem in which a calculator is used.

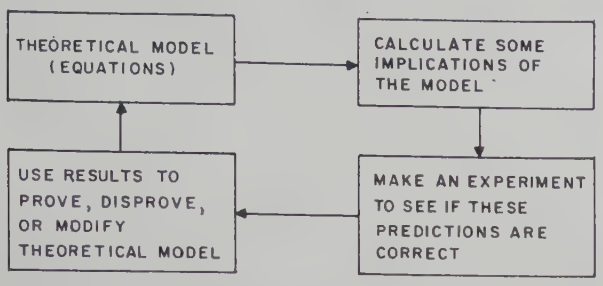

Fig. 1—Typical method of solution of a research problem using a calculator.

We start with a mathematical statement which is supposed to represent some part of the jet engine or some part of the brain. By mathematical processes we determine some things which this original statement implies. Then we check to see if these predictions are in fact borne out by experiment. Finally we use the comparison of theory and experiment to prove, disprove, or improve the theory.

One of the theories which has been advanced as to how the brain works was put forth six years ago by Professor Hebb at McGill University.[1] In this theory Hebb attempted to bridge the gap between psychology and neurophysiology. This is a bold effort since the gap is large. In fact, Hebb states in his book that it is significant that it seems possible to describe a theory which bridged the gap, was consistent, and did not violate any firmly established laws of neurophysiology or psychology.

Fig. 2 is an idealized version of Hebb's theory. What I have chosen to call Theorem A is an assumption about the behavior of neurons. This assumption is alleged to imply Theorem B, which I will describe as relating to the formation of concepts. This is alleged to imply some things about behavior which I will call Theorem C, and which can be tested against established psychology.

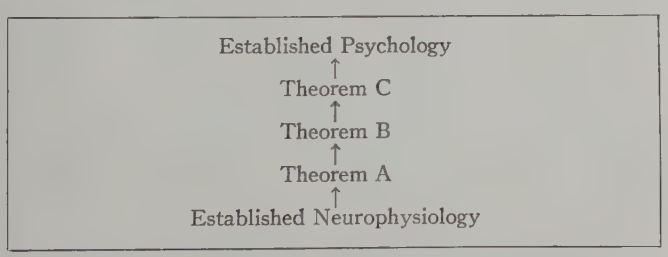

Fig. 2—Idealized purport of Hebb's theory.

It appeared that by using simulation on the IBM Type 701 we would be able to test the transition from Theorem A to Theorem B. When we attempted to do so the first thing that we ran into was that the theory was not quite definite enough, so we had to make a few additional assumptions. Having done this, we found that Theorem B did not follow from our specific version of Theorem A.

While this was going on, some other people, including Dr. McCulloch's group, had proved some new things about neurophysiology and Theorem A was inconsistent with these.

The original theory is too vague, details seem inconsistent, and seem to contradict observation. However, with one of Hebb's students we have reconstructed part of the theory to get around all of these troubles and are ready to have another go at it.

This is just about what we expected. There isn't time to describe the neurophysiology in detail and explain this important matter about how concepts are formed, but I can give you some idea of what it is all about.

First of all, consider the time constants. If one neuron fires and stimulates another, so that the second neuron fires, the second neuron will fire about one millisecond after the first. Therefore, we have one time constant of one millisecond. It is the primary time constant of the elementary units of which the brain is composed, the neurons.

Now if I count out loud 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, it takes me about three seconds, but if I count to myself—the way you did when you were a child playing hide-and-seek—just as rapidly as I possibly can, it takes about one second. Thus a single digit has a time constant of at least 100 milliseconds. A kind of delay-line memory appears to be the connection between these two time constants.

It is apparently not the kind of memory shown in Fig. 3, which is presented to orient your thinking so that you will think about the correct aspects of the next two figures which illustrate how the brain may do it.

Fig. 3—A one-dimensional chain of neurons—*not* the way the brain remembers.

If 100 neurons were connected in such a fashion with sufficiently strong connections from one to the next, it would be possible to put a signal in at one end and it would fire neuron N_1 first. About one millisecond later, neuron N_2 would fire. One millisecond after that, the next neuron would fire. After 100 milliseconds the last neuron would fire. Therefore, this structure would have the necessary 100 millisecond time constant; but probably the brain doesn't do it this way.

In Fig. 4 there are seven neurons, and each sends signals to three others. If we had 10,000 neurons, each connected to one hundred others, we might be a little closer to what some people suppose to be a detail of the brain structure. With the Type 701 Calculator, we have

[1] D. O. Hebb, "The Organization of Behavior," John Wiley and Sons, New York N.Y.; 1949.

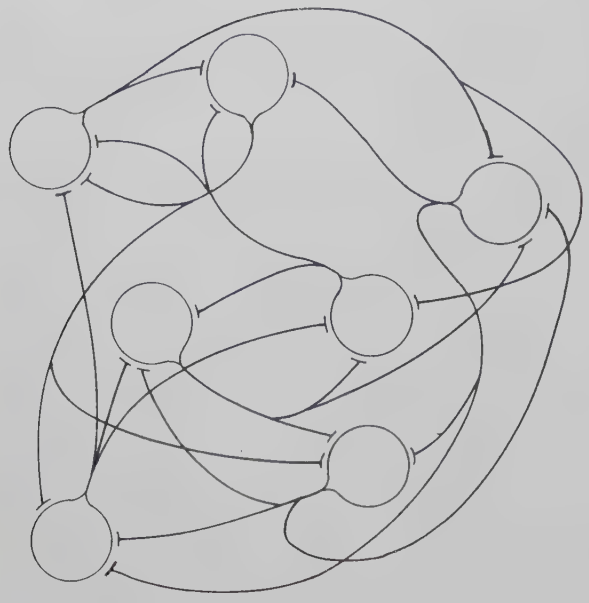

Fig. 4—A distributed poly-dimensional assembly of neurons—typical of the brain's supposed structure.

made experiments with sets of 63 simulated neurons each connected to about eight others, and a typical result is shown in Fig. 5. The net was initially quiescent, and a few neurons were fired from outside. Then the activity reverberated in the net for a time equivalent to about 150 milliseconds before dying out.

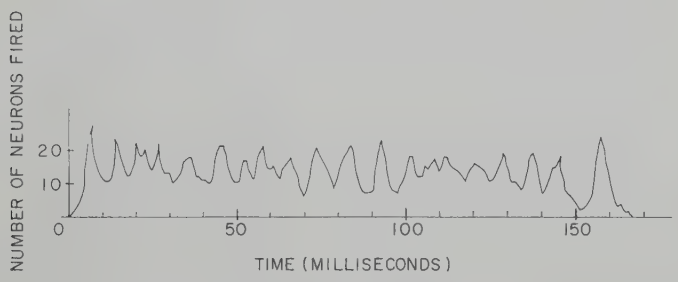

Fig. 5—Response to an initial stimulation by an assembly of 63 neurons, each connected to 8 others, as simulated on the IBM Type 701 Calculator.

This kind of diffuse reverberation appears to be a possible mechanism for controlling serial order in behavior. It also appears to be a possible mechanism for short-term memory in the brain. By short-term memory I mean, for example, the memory which retains intermediate results when one is working out a problem in arithmetic.

Professor Hebb called an interconnected net of such cells a "cell assembly." A cell assembly can be aroused, as it is here, or quiescent as it was before or after. At any instant the brain contains a large number of aroused cell assemblies and a very much larger number of quiescent cell assemblies. Mental activity consists of a kaleidoscopic sequence of aroused cell assemblies.

In conclusion, I would like to say that it appears to be possible to use modern automatic calculators to test some aspects of some of the theories of how the brain works. No other tests of these aspects appear to be available and the signal levels in the brain are so low that it may be many years before tests can be made by direct measurement. Therefore, we expect that we will be able to contribute to man's understanding of the brain. If this casts any light on the problem of how to make a calculating machine, as it very well may, it will be another example of the indirect benefits of research.

The Brain as a Different Computer

Otto H. Schmitt: It has become a popular sport in the past few years to describe brain functions in computing-machine terms and computing-machine functions in human behavioral terms and to get a good deal of satisfaction out of the notion that while it may take a year or two yet, we will certainly be able to understand mental function in computer terms before too long and will shortly thereafter be able to design really heavy-duty brains with greater speed and capacity, and increased reliability.

While I am all in favor of such enthusiasms, on the basis that nothing succeeds like success, I believe I should risk the disapproval of some members of this group of investigators by pointing out a type of circular reasoning which has been prevalent in their arguments. This is the fault of using a disguised form of an hypothesis to prove the hypothesis.

To illustrate my point, I would like to tell you a true story about one of my colleagues whom I shall not name. This gentlemen, a professor of considerable fame, was waiting to listen to a fight on the radio but because the fight was delayed in starting, he idly turned to the university station and heard a lecture already in progress with which he became very impressed, and to which he listened most attentively. Because he agreed so completely with the speaker's point of view, he availed himself of the invitation at the end of the lecture to send a postcard for a copy of the lecture. He was considerably taken aback when he received his copy to find a note attached asking whether he had lost the original copy as he himself had recorded the lecture on tape several months ago for later broadcast.

By analogy with this story, I believe we have fallen into the trap of describing some brain functions in terms of present-day computer components and are then delighted to discover machine-like components in our description of brain function. I do not mean to belittle the pioneer attempts of Rashevsky,[2] Hebb,[3] Culbertson,[4] Ashby,[5] and many others;[6–9] and indeed I should con-

[2] N. Rashevsky, "Mathematical Biophysics," University of Chicago Press, Chicago, Ill.; 1948.
[3] D. O. Hebb, "The Organization of Behavior," John Wiley and Sons, New York, N.Y.; 1949.
[4] J. T. Culbertson, "Consciousness and Behavior," Brown, Dubuque, Iowa; 1950.
[5] W. Ross Ashby, "Design for a Brain," Chapman and Hall, London, England; 1952.
[6] J. C. Eccles, "The Neurophysiological Basis of Mind," Clarendon Press, Oxford, England; 1953.
[7] J. Z. Young, "Doubt and Certainty in Science," Clarendon Press, Oxford, England; 1951.
[8] L. L. Whyte, ed., "Aspects of Form," Lund Humphries, London, England; 1951.
[9] L. A. Jeffress, Editor, "Cerebral Mechanisms in Behavior," John Wiley and Sons, New York, N.Y.; 1951.

gratulate two of our other speakers on their success in this field. Warren McCulloch and his associates have gone a long way to associate digital-computer significance with known brain functions, and Mr. Rochester's account of an attempt to document Hebb's theory is very interesting.

I believe, however, that we are taking an unbalanced view of the problem, based on the phenomenal success of the large digital machines, and are thereby depriving ourselves of a tremendous complementary development of more brain-like machines.

Digital computation is based on the nice clean notions of precisely defined concepts, and of operations which can be carried out with unlimited precision to give results of unlimited accuracy. Admittedly, the machines can be told to stop after so many approximations, or to throw away data beyond the thirteenth decimal point, but the idea is inherent that the machine itself should always know right from wrong, black from white, if it cares to go to the bother of thinking about it.

In the biological world of hot competition for survival, as in engineering, which also has its battles of survival, the criterion seems to be one of choosing a computation means just a little bit better than good enough to do each of the jobs at hand, and to use any superfluous energy, time, space, or self-duplicating ability to build up a little extra reserve in all departments.

If we care to think of this biological economy-for-survival-and-ultimate-progress principle as a guide, we should treat as suspect any design which seems to display tremendous reserves of precision, or storage capacity, or flexibility, and should ask whether the job couldn't be done more cheaply or more simply, or the machine utilized more completely. In effect, we should doubt whether high-powered loafers, animate or inanimate, are a good thing.

Now, following up my original claim that present-day digital computers are hardware embodiments of elementary-school-book black-and-white logic and of the associated formal operations of basic mathematics, I must presumably offer some neurophysiological evidence on which we can base other less logical but more intelligent computers which will ultimately extend the speed and range of our reasoning power, as present-day computing machines are extending our adding-machine capabilities. This it is easy to do, for the cream has not yet been skimmed from the last century of physiological experimentation, with its accompaniment of correlated psychological, neuro-anatomical, and homeostatic studies. I will not even exhaust my own meager stock of information but will cite only a few cases.

First, there are the behavior properties of the neuron itself, which only in very special cases correspond to purely digital information-manipulating concepts. The neuron has a most interesting mixed pulse code which is a combination, in each single channel, of the function itself, of the time derivative of the function, and of the function time integral, in proportions which are permanently adapted according to the task the fiber must do, and temporarily modifiable in terms of the recent work load. This very untidy mixed code turns out to be most efficient in transmitting and manipulating information of the really important sort; that for example, which tells the state of affairs these days, what's been happening lately, and what's to be done about it right now. It is an admirable combination of neural code and computer code.

Next, there is the smooth transition between a digital place-code and an analog magnitude-code, which is found everywhere in the central nervous system and its periphery. The nervous system can with great facility run successive approximations, with a substantial safety margin in each run. This is the strong point of place-register-type computers. But the nervous system can also, by almost imperceptible degrees, exchange item safety-factor for channel capacity, to permit a flexible compromise between being right and yet having some kind of an answer at all times. Unlike conventional computers, this type of operation leads toward solutions which are roughly formulated almost at once, and are then constantly improved by refinements and increased precision.

As you see, this type of operation leads to a statistical, distributed kind of computer, where items are seldom stored specifically in any one place, and where preforms are omnipresent and constantly important, but never take the form of nice crisp tables or tapes. But with the short time available, I must not belabor this "grey-logic" aspect unduly; there are other physiological data in abundance which must be utilized in our brain computer for they are known to be present.

One of the most interesting and singularly unexploited nervous-system properties is the decision-forcing property which arises from the negative-resistance characteristic of the living cell. Dr. McCulloch spoke of this characteristic in somewhat more simplified terms as a progressive short-circuiting, which makes the electrical nerve impulse propagate. When we realize that this characteristic actually is a time-variable negative resistance, we understand how the cell can take a kind of census of the opinion of surrounding cells and then act decisively. It can also force synchronization over a narrow time-place region but reject identification outside it.

There is also coming to hand more and more data[10] which suggest that the negative-resistance characteristic is not a steady comfortable negative resistance like that of fed-back tubes or transistors, but more like the gas-discharge-tube characteristic which tends to flutter and undergo random fluctuations. It is perhaps permissible without demonstrable evidence to see in this random "playing," which is now well known in biological cells, the basis of imagination and initiative in computers; for example, the willingness to bet on a likely solution even if not fully justified, a desire to try something a little different, the recognition of a slightly far-

[10] O. H. Schmitt, T. Shedlovsky, ed., "Electrochemistry in Biology and Medicine," ch. 6, John Wiley and Sons, New York, N.Y., and Chapman and Hall, London, England; 1955.

fetched analogy even if not perfectly documented.

In conclusion, then, I look forward to the development of grey-logic computers with statistically formed decisions, neural-synchronization type of automatic correlation and recognition of correlation, and flexibility of components. I also anticipate codes utilizing combined time-and-place localization of data, with very rapid access to logical preforms, each of adjectival modifiability. I am not certain, either, that we will not find new biophysical laws of behavior for highly organized computer systems of the above type which will extend the importance and the capabilities of such computers enormously.

I hope that I have not been too sweeping in my résumé of the type of brain-like computer which I envision. I fully recognize that we must fumble along brick-by-brick in building this ideal, first building a little better idea of the brain, and then building a little better machine based on that concept, from which we will again and again be able to make further approximations.

I have avoided spelling out in detail the volt-ampere and millisecond details of nerve synchronization, interrogation, display, correlation, et cetera, but I shall gladly elaborate on any of these details insofar as my technical knowledge will serve, and I am sure that other members of the panel will have many items of information which I lack. Thank you.

Discussion by the Panel

H. E. Tompkins: I am now going to ask the panel to discuss the topic of our symposium, and would like to begin by asking Dr. Schmitt to define one term which I did not understand fully. What is a "preform" as it exists in an organism?

O. H. Schmitt: I use this term "preform" to represent the numerous stylized but slightly flexible patterns of behavior exhibited by the animal or man in response to characteristic combinations of cues, or of nearly equivalent patterns of cues, even if presented in varying sensory modes. These preforms, some innate and some learned, are set in motion by key combinations of stimuli, sometimes called releasers, and are usually very efficient means to a practical end, but occasionally lead to systematically repeated blunders. These preforms are the biological counterpart of automatic subroutines built into computers, such as recorded function tables and the like, but differ markedly in their combination rules and simultaneous compatibility. Subjectively we experience these preforms as "ideas," "principles," "approaches," "ideals," "prejudices," "intuition," and "skills."

Chemical Action, Too

N. Rochester: I would like to ask Dr. McCulloch a question. The neurophysiologists once thought that maybe nerves were pneumatic in function, that they conducted air pressure around, and this is how muscle is controlled. As science progressed the neurophysiologists took over newer and better technology from the physical sciences for their conjectures, and every once in a while it turned out that one of these conjectures was right. What I wanted to know was whether it looks to you as if we have enough techniques around now to explain the brain, or whether a lot more techniques will have to be developed?

W. S. McCulloch: I doubt very much whether we have all of the necessary techniques to understand the working of the brain. The chemical aspects of its activity can only be detected in a few cases by decent electrodes whose surfaces are responsive to one or another components in the tissue, say, the hydrogen ions or the pressure of chloride ions, and so forth. We have none of the nice devices which the nervous system seems to enjoy for tasting. One is phosphate electrodes. Brain seems to handle energy by the triphosphate bond, apparently as energetic as any bond it can make or break at ease. I have no doubt that a good phosphate electrode would push us ahead fairly well.

To say that our tools are not adequate for us to follow electrical disturbances is not strictly correct. Practically, in a sense, they are. We have electrodes small enough to be actually in the cells. We can make them very easily to sample the ground around the nerve cells, and so forth. By various means, we are able, at least for statistically significant contemporaneous activity of neurons, to detect where impulses are, whence they came, and whither they are going. Consequently, I am sure that while other techniques may come in to supplement those that we have today, we will never again suffer the grand revolution that we did when we had to give up hydraulics for electricity.

H. E. Tompkins: It may come as somewhat of a surprise to the electrical engineers that a substantial amount of the brain's activity is not electrical in nature. Can you comment on this balance between electrical and nonelectrical brain action?

W. S. McCulloch: Well, the brain must have energy enough to keep its battery charged. Over and above that, it must have enough energy to keep itself in shape, because things in the shape of a neuron don't persist in this world without expenditure of energy. It doesn't have to have energy for reproduction after it has once laid down its neurons, because they don't reproduce. On the other hand, it has all kinds of cells dying and they have to be gotten out of the way. So there is a good deal of chemical activity. So far as the over-all activity is concerned, its business being with signals, all it can do with most of the energy that it handles is to dispose of it as heat.

O. H. Schmitt: Dr. McCulloch's remark reminds me of one characteristic of brain behavior for which I believe there is no obvious computer analog. Many chemical agents, including particularly a number of specific hormones and alkaloidal drugs, enter into the control of brain function in a sidewise fashion, for they change the

functional characteristics—sensitivity, time constants, etc.—of multitudes of cells throughout the brain, thereby altering its over-all behavior patterns tremendously, but do not *per se* contribute at all to the nerve impulse pattern.

H. E. TOMPKINS: Is not this sort of thing analogous to a change of the power supply voltage in an electronic system?

O. H. SCHMITT: Not really. In the body the modification of brain function is purposeful, and more like the action of a set of frequency-selective agc circuits governed by an all-pervasive control frequency in itself devoid of explicit message content, rather than like a change of supply voltage.

CELL ASSEMBLIES

H. E. TOMPKINS: Dr. McCulloch, I would like to ask if research with your microelectrodes has gone far enough that you can establish this cell assembly theory that Nathaniel Rochester discussed? Is it true that cells are grouped in these assemblies?

W. S. MCCULLOCH: These are to be thought of as transient associations. No, our techniques are not of that specific kind. It would require a great number of electrodes of minute size stuck into a fortunate combination of cells in just the right part of the brain before you would expect anything that could even look like these cell assemblies.

N. ROCHESTER: I think that is right. I didn't mention this before, but the cell assembly is visualized as being distributed quite widely in space. Any theory must be consistent with the experimental fact that you can remove a lot of brain tissue without damaging the animal very seriously. You have to find some mechanism which would be invariant with respect to removing nine-tenths of certain tissue, but not invariant with respect to removing 100 per cent of it. These cell assemblies could be all mixed up with one another, spatially. Then an excision would remove parts of a lot of cell assemblies, but each of the cell assemblies would still exist, with a reduced number of participating cells.

H. E. TOMPKINS: You described the cell assemblies as transient associations. Do you mean that the physical connections are changing, or are interchanged, one with another?

W. S. MCCULLOCH: Not that their anatomically fixed components are necessarily changed, but that activity in some other group of cells ties up with this group in one place on one occasion to excite it, or to inhibit it on another occasion. Which groups are associated at any given time changes, much as the clusters of signals in a computer change. The cell assemblage would be one determined possibly by the program.

WHY BUILD A MACHINE "BRAIN"?

A. G. OETTINGER: I have a question to address to Dr. Schmitt. You talked about the desirability of designing a machine which would operate in what you call a "grey logic" rather than in a "black-and-white logic." Now I am confused about what the purpose of such a machine is. If it is to demonstrate that a machine designed along principles of this kind can give a realistic simulation of brain behavior, then I can see this may be useful.

If, however, such a machine is intended as a tool to amplify our physical and mental powers the way our other machines do, then I am a bit doubtful about its value. As a tool, the human mind has certain limitations—it is slow, it gets tired, its attention wanders—which is precisely why we built machines to help it. To build machines with precisely the powers and the limitations of the human brain would not seem helpful or economical, considering how many generations of people it took to get us to our present state of knowledge. Furthermore, we are doing rather well so far as the production and supply of this type of machine are concerned, so why build one out of hardware?

O. H. SCHMITT: I am quite happy to elaborate on that point because I believe it is central to my argument. Even strictly on the basis of economics, it is necessary to abandon the idea of perfectly correct, uniformly logical solutions in any machine which is to arrive at generally appropriate quick solutions to complex problems when provided only with sketchy, conflicting, and partially inappropriate information and instructions. For such work present-day computer elements are hopelessly ponderous and stupidly logical in their need for precise programming, and in their lack of imagination.

The simple decision as to whether it is advisable, at a particular time and place in the road, to exceed the established speed limit is one that would be most difficult for a machine to make without inclusion in it of a great deal of tradition and factual information, and some personal opinion. The strength of the human brain in this situation lies in the human's ability to make a decision promptly and forcibly on the basis of inadequate evidence, to carry through on the basis of these decisions as though they were axiomatic—unless forced to modify them—and to be successful at doing all this.

If we can successfully extend to machines the ability to make decisions on an experimental basis, utilizing to the full any available inadequate evidence, and then extending and expanding this decisiveness as additional data come in, we will be far ahead of someone else who designs machines which must operate on specific instructions.

IS SYSTEMATICNESS UNDESIRABLE?

A. G. OETTINGER: Let me ask you this. Supposing that you want to do this—to get a machine that will make decisions under conditions where it does not have full evidence—why is it necessarily implied that a machine then has to have a certain element of indeterminacy? Why can't a machine *systematically* make decisions on insufficient evidence?

O. H. SCHMITT: In order to achieve greatest effective-

ness, it must systematically put in nonsystematicness. One can, of course, put in randomness systematically, but perhaps it is to be had more cheaply by letting in a bit of carelessness. By such randomization, with feedback checks of results, you can, in general, outguess the systematic machine and can do it at lesser cost. Probably it is by this kind of process that we get answers to difficult problems: we go to a point known to be in the vicinity of a solution, and then feel about and lash out blindly until we chance upon a solution.

A. G. Oettinger: That may be characteristic of a poker game or of any situation where you are trying to get at your opponent. But what I wonder is, if you are trying to use a machine as a tool to do something for you that you can't do yourself, it seems to me that if the machine turned back on you and decided to outguess you . . .

O. H. Schmitt: Your other employees should try to persuade the machine to guess with you rather than against you.

A. G. Oettinger: What happens is a very nasty problem of communication. Supposing I have a machine and it decides to switch at arbitrary time intervals from giving answers in English to giving them in Russian and vice versa?

H. E. Tompkins: Perhaps at this point we need a definition as to what we mean by "systematic nonsystematicness." How do you make this randomness systematic? What does this mean or imply?

O. H. Schmitt: In one case that I might talk about, it would imply that a cell would play about in a relatively random fashion as to the exact threshold at which it was going to decisively go ahead or not go ahead, but that it would not do this in any contrived fashion.

H. E. Tompkins: This does not seem to be systematic. You used the phrase "systematic nonsystematicness." How does that differ from just plain nonsystematicness?

W. S. McCulloch: May I jump in on that? I would like to ask a man who is thoroughly familiar with what computing machines are used for whether he doesn't do just that trick on certain occasions, as the best way to solve his own problem; I mean that he feeds in random numbers even if it is difficult to compute random numbers?

N. Rochester: Yes, I think that is right. What you are referring to is the Monte Carlo method. But there is something there you have to be careful about. In putting numbers in, you have got to be careful so that they are really at random, for if they aren't they will help you to influence the answers the way you want them to come out. One of the things that the experts have put a lot of time on is the theory of how to generate random numbers which are really very random.

H. E. Tompkins: In the Monte Carlo method, do you use a sequence of random numbers to search truly randomly for a solution; or is this a gross simplification of what the method actually is?

N. Rochester: In some applications, Monte Carlo is used in this way. There are a lot of possibilities as to what might happen, and there are so many that you can't set up an equation for each possibility. Therefore, you start off at random by playing a game and the machine chooses possibilities in accordance with an appropriate probability. From the result of the experiment you get a rough idea of what the answer probably is, and from this guess made for you, you may be able to formulate a better and more exact statement.

H. E. Tompkins: Does the machine do this formulating or do you?

N. Rochester: It sorts through a lot of possibilities and finds one that would be the most likely.

A. G. Oettinger: Yes, but it does this according to the criterion of likeliness which has been definitely built into the computer program! It seems to me that it is in this respect that the Monte Carlo method differs rather significantly from what I think Dr. Schmitt had in mind. While we may put in a white noise generator, or something to get random numbers, there is one restriction already implicit there—that what we want at random is random *numbers* and not random *words*. Certainly not random connections in the machine, and eventually random interchange of input and output, and so forth. In connection with this, what happened here before in this room, with the controls for the microphone and the lights and the slides getting mixed up, is an example of what happens when uncontrolled randomness gets into a situation, or into a system. The microphone, slides, and lights ceased to be useful tools!

Growth as a Type of Learning

O. H. Schmitt: There is a feature of the design of biological organisms which I believe should be emphasized at this point: namely, that each individual arises out of a single-cell stage where most of its design information must be compressed into a very small, highly ordered package, and hence in a state of low randomness. In all probability the individual items of genetic instruction are carried at energy-difference levels of the order of kT, and hence with high informational-content efficiency but with relatively low item security.

Apparently important genetic features are secured through moderate molecular redundancy and are systematically randomized through the usual chromosomal interchanges, but immaterial design factors are not very tightly specified, but are only gently directed through embryology and growth. The result is a very reliable but somewhat varying product nearly always having all important features and sometimes having individually distinct good or bad features which mark the individual product for success or extinction.

Unlike ordinary computers, therefore, the biological organism is built on a vast trial-and-error basis, with only the high points of its development guided. From zygote to mature individual the biological organism modifies its design as it goes, and by this "learning" process achieves outstanding success at goal-seeking and

problem-solving activities at which computers are signally inept.

A. G. Oettinger: In that sense, the organism is restricted to relearning, each generation anew, the knowledge accumulated by the preceding generations. But with computers, it seems to me that we are able in principle, by the use of appropriate programming or designing of structure, to build in one swoop the whole background of explicit existing knowledge. It seems wasteful to build a machine to repeat the trials and errors made by untold numbers of human brains in many thousand years.

O. H. Schmitt: But computers don't do any particularly profound operations. Suppose that you wanted to throw into the machine a democratic process, or that you want to insert the knowledge of what democracy is, into a computer: would it not be impossible? It would certainly be very difficult.

H. E. Tompkins: On this point of saying that we are able to build knowledge into a computer, with the present state of the programming art as it is commonly applied, I wonder if we really can. As it stands now, a program prepared for one problem on one computer is transferable very, very little to other problems or other computers. The current development of many automatic programming techniques may have a significant effect here.

Now, I think we should close off this first part of the discussion and call a brief intermission. I will then ask our invited panel questioners to come up to the platform, and we will have the second half of our symposium.

Questions and Further Discussion

H. E. Tompkins: Our questioners have taken their places on the opposite side of the platform. I would like to introduce them briefly. From left to right they are: M. L. Minsky of Harvard University; Morris Rubinoff of the University of Pennsylvania; Elliot L. Gruenberg of the W. L. Maxson Corporation; John Mauchly of Remington Rand; M. E. Maron of IBM; and Walter Pitts of M.I.T.

I don't have any built-in preforms as to which questioner should go first, so let us see who really wants to begin; Mr. Maron!

What Does Simulation Prove?

M. E. Maron: I think that one could use the language of the computer engineer and make the following analogy. One could consider the brain as a "black box" and say that it is the task of the neurophysiologist to attempt to analyze what exactly is in the "black box." Due to the complexity of his task the neurophysiologist is, at present, unable to provide us with circuit diagrams. Even if he could, we don't have any suitable components at our disposal and therefore we cannot consider building a brain in the sense of connecting components according to the neurophysiologist's circuit diagram.

An alternative way to attack the problem of understanding "brain behavior" lies along the lines followed by the behaviorial psychologist. In a sense, the psychologist looks only at the inputs and outputs of the so-called "black box" and attempts to obtain as complete a description as possible of the inputs and corresponding outputs without regard for components or their wiring within the box. It has become fashionable (and true) to assert that given a complete and unambiguous description of the behavior (*i.e.*, inputs and outputs) of a device one can (in principle) build another device (or program a computer) which will behave in a corresponding manner.

Again, in the case of the human brain, no psychologist, at present, is able to give a complete description of its behavior and I would conjecture that no psychologist will *ever* be able to provide such a description. (Perhaps my feeling about this stems from the paradoxical fact that such a complete description of a brain would have to include a description of how a brain attempts to understand another brain, and so on *ad infinitum.*) Again, since the neurophysiologist cannot provide a wiring diagram of the brain and since the psychologist cannot supply a complete and unambiguous description of its behavior one might consider another way of simulating brain behavior and this is the method described by Mr. Rochester. Mr. Rochester has programmed the 701 so as to have it copy the behavior of certain neural networks. That is to say, his approach is to continually modify his computer program until he can get it to respond as it appears that neural networks respond.

Now, my question for Mr. Rochester is this: Assuming that one can formulate a computer program so as to simulate the behavior of a neural network—what legitimate inferences about the brain can be drawn from the computer program in question? Or, to state my question differently: Given an arbitrary model of a brain whose behavior does not contradict what we know as actual brain behavior, what inferences can be made about the actual make-up of a brain on the basis of such a model?

N. Rochester: Well, one answer might be this. Professor Hebb has provided a tentative theoretical structure bridging the gap in our understanding lying between neurophysiology and psychology. If the model which represents the theory works as he says it should, the experiment would give support to the theory. Of course it would not prove that the theory correctly represents living tissue. On the other hand, if the model does not work as expected it might force modifications in the theory. I regard these experiments as pure research. I am trying to find things out. I got started in this direction because I wondered why people can do some of the things that machines can't.

The Semantics of Reproduction

A. G. Oettinger: That last point is very often

purely a matter of definition. There is something that I have been itching to toss into the record here, with regard to the problem usually raised about the possibility of machines reproducing themselves—something that they are alleged not to be able to do. This question was very well treated by Samuel Butler about 80 years ago.[11] I would like to quote what he said regarding this.

> "Surely if a machine is able to reproduce another machine systematically, we may say that it has a reproductive system. What is a reproductive system, if it be not a system for reproduction? And how few of the machines are there which have not been produced systematically by other machines? But it is man that makes them do so. Yes; but is it not insects that make many of the plants reproductive, and would not whole families of plants die out if their fertilization was not effected by a class of agents utterly foreign to themselves? Does anyone say that the red clover has no reproductive system because the bumble bee (and the bumble bee only) must aid and abet it before it can reproduce? No one. The bumble bee is a part of the reproductive system of the clover. Machines can within certain limits beget machines of any class no matter how different to themselves. Every class of machines will probably have its special mechanical breeders, and the higher ones will owe their existence to a large number of parents and not to two only."

With regard to the question of defining what machines can or cannot do, I suggest that a careful inspection of Butler's witty discussion of this problem be made.

E. Gruenberg: For some reason, I can't get too enthusiastic or interested in reproduction being done by machines. I do feel, however, that perhaps there is some definite value in learning lessons about how to design machines from studies about the structure and neurophysiology of the brain, as mentioned here.

Where Is the Memory?

E. Gruenberg: I was particularly disappointed, when I read about the Hixon Symposium of 1948, that they didn't know where the memory is. This, I think, is an important part of the whole problem of learning how to make machines more versatile. I was wondering whether Professor McCulloch could tell us whether there has been any more progress in finding out where the memory is, and what might account for the different types of memory that seem to be displayed by the human being. For example, some seem to store up all kinds of facts and they don't seem to put them together too well, and others seem to have just a few facts in memory, but they seem to put them together with amazing facility.

W. S. McCulloch: I think the simple fact is that I am not the right man to answer the question. The right man isn't here. He is J. Z. Young. He is a Professor of Anatomy in London who went to work not on man, but on the octopus!

The octopus carries his very short-term memory around in his ordinary computer. Then he also has a nice large globe of small cells, and channels for access to it and proper channels of egress from it, and in this he carries his long-term memory. So we do know in the case of the octopus not only in which part of his brain his long-term memory is stored, but we are beginning to know something of the wiring diagram thereof. The difficulty is one of finding good methods of staining the particular components in the octopus, so they can be observed adequately.

M. L. Minsky: On this question of where information or memory is stored in the nervous system, I would like to ask Dr. Schmitt to what extent he thinks we have been getting the kind of knowledge we need. When you have a computer, it is not usual for people to ask what metal it is made of. Granting that we do not know all we might like to about the metabolism of the cell itself, it would still be very nice if we knew more about the manner in which information is carried from cell to cell. This type of information is really necessary, and could not one hope to build up much of brain theory using primarily this intercellular data without needing a great deal of intracellular data? I would like to have your estimate on how much knowledge will be needed before we can go about analyzing the interrelation between cellular properties and the over-all properties of brain.

O. H. Schmitt: We like to work toward the descriptive information you ask for by doing two different types of experiment. Since we know so poorly how the individual units function, we test them individually for their chemical responses, their electrical characteristics, etc. Then we experiment with the composite group to determine its over-all behavior insofar as possible being sure to preserve the integrity of the analysis by not postulating, in our description of group behavior, characteristics contrary to the findings on individual units.

Don't Preclude a Different Answer

M. L. Minsky: Dr. McCulloch mentioned that we would like to stain these fibers in some nice manner. I feel that it is important to know the ways in which the cells are interconnected. If you worked on microtechniques from this point of view, it seems to me you might be able to go far with that information. There seems to have been very little work done in this direction.

O. H. Schmitt: I think you demonstrate by your question a difficulty into which we, as theory makers, have frequently fallen and from which there is no easy escape, namely that of precluding solutions other then those which happen to occur to us.

You are assuming in your question about interconnections that the nervous system must be a net of the telephone-switchboard or conventional-computer type where messages of a particular significance are pre-

[11] Samuel Butler, "Erewhon, and Erewhon Revisited," Modern Library No. 136, ch. 24, Random House, New York, N.Y.; 1927.

dominantly channeled through a specific line and can thus be sharply localized at any specified time.

In all probability the central nervous system including its memory and computing functions is a widely distributive statistical time-place-state system where memory of a particular event is smeared out over some millions of cells and these same cells simultaneously hold many millions of other memory traces. You could spend your life looking for a single memory trace as an altered state or connection of some particular cell without success, yet the trace would be there, spread out over the mass of cells as a slight disturbance of the over-all patterns of response in time and space. In such a system the storage capacity of a few millions of cells becomes astronomical.

What I believe we must find out are the general rules of actual behavior for the individual cellular components, for the small aggregates of components and then for the whole systems of neurons, so that we can stop describing brain action in terms of neural networks which are physiologically and neuroanatomically unreal and can substitute actually feasible schemes—no matter how bizarre they may seem in conventional switchboard terms.

"Distributed" Memories

M. L. Minsky: It may be true that we must conceive of memory as widely distributed in some sense, but I don't think we can work scientifically with an idea like that until it is clarified by the availability of an assortment of models to show how this might work. There may be lots of ways of doing this but I feel we will have to be more specific in our models before we can direct experiments in this direction.

N. Rochester: We don't have models, but we have experiments to prove that the memory is distributed in some very wide fashion.

W. S. McCulloch: A psychiatrist[5] has invented a model in which the memory is so distributed; that is, the thing you have to look for, and where you have to look for it, are dependent upon the sequence of the events in that particular learning sequence, and the changes are not localized in any sense to any one component.

A. G. Oettinger: You can't point to any single element in that circuit that remembers the single state of the circuit. The state is distributed over the whole system.

M. L. Minsky: The Ashby model doesn't distribute anything at all so I don't see how it can be considered as a model for a distributed thing. This model starts wholly anew after each act, and has no memory at all of its previous states, distributed or otherwise. It is true that it has impressive properties in the direction of functioning well after damage to any of its parts.

It seems to me that the idea of "distributive memories" has come to refer to two different kinds of models, with a continuum of intermediate types. First, there is the type suggested by Hebb, for example, in which a piece of information is stored in a reasonably small assembly of entities, but with the location of these entities widely distributed spatially. If such a piece of information were related to the occurrence of a very few neural events but these were spatially separate, that would still explain the difficulty of locating the data in the brain by physical stimulation techniques. And if this information were duplicated in the brain just a very few times, that would explain the resistance of memory to injuries involving damage to large portions of brain. The other notion that is current is that which Dr. Schmitt has just expressed; memory is held in the form of very, very small changes spread over millions of cells. I have no quarrel with this idea, and would be delighted to see a model which works this way. But no one seems to have been able to indicate how such a thing might work.

W. S. McCulloch: Another difficulty hinges on this: A black box like the human brain has one millisecond access time to it over approximately three million channels. It has an output every one millisecond over better than a million channels. How much output information would you need—how many observations would you have to make—to have a thorough knowledge of the input and output? The universe hasn't particles enough to record it.

Memory Half-Life

J. Mauchly: I had several things to ask. I want to hark back to some of the very first things that Dr. McCulloch said. I was puzzled by the statement that some of the human memory had a half-life of something of the order of half a day. What is meant by this, and how was it discovered?

W. S. McCulloch: It was evaluated quite a few years ago by a careful group of psychologists studying a good variety of inputs of human beings, and seeing how long they were retained—things like nonsense syllables fairly well equilibrated, and so on. I am not proposing that the result is anything more than a general guess. Nor does it cover that small per cent which one retains by some sort of process of rejuvenating it inside oneself. If you know a certain number of facts here and now, within twelve hours you will have lost half of them. There are fairly good curves available on carefully selected subjects. I don't mean to say this is characteristic of all mankind, but it is characteristic of selected people reading the test items in question.

Now, this is not the only kind of memory that a man has. This kind of memory is characterized by getting better every time you repeat the item. There is also a certain kind of memory which one has that works much more like the acquisition of skilled acts, a memory which gets better when you let it rest. You use it and use it, and then let it rest, the way you train a muscle. This provides quite a different curve of performance on tests. The third kind of memory one has is of a problem while it is still churning in one's head, the kind of char-

acteristic memory that is left to a very, very old man.

H. E. Tompkins: And then, finally, is there not a long-term memory, which is something else?

W. S. McCulloch: The long-term memory is apparently some process which keeps reproducing traces. I see Heinz von Förster in the audience, and I think he was the first man to clear up this theory.

J. Mauchly: I noticed a reference to the octopus having two kinds of memory, and now listening to the most recent answer, it sounds as if we are distinguishing between at least three characteristic memory spans, half-lives, or something in the human memory. Are these really clear-cut?

W. S. McCulloch: These three are reasonably separable and capable of being distinguished from one another.

Analog vs Digital

M. Rubinoff: I get the impression that the word computer bears the connotation of digital computer. The talk about relays and circuits and general-purpose computers is digital-computer terminology; however, in Dr. McCulloch's talk, and in some of the writings that appear in the periodicals, it appears that the brain and the nervous system use both analog and digital processes. I wonder if Dr. McCulloch would care to comment on the areas allocated to the two different modes of computation or processing, if you want to call them that; and perhaps if he cares to, on the relative efficiencies of those two modes in the areas where they are used. Perhaps I could say, how well has the human being been built; have we had our analog parts, and so forth, put into us in the proper proportions and the proper ways to make really good processors out of us?

H. E. Tompkins: Perhaps we should refer that to Dr. Schmitt.

O. H. Schmitt: The answer to this question is not that here we have a digital system and there an analog system, but rather that most everywhere we have a simultaneously functional mixture of the two, and the distinction is semantic rather than functional. Let me illustrate with an example from the acoustic sensory transducer system in an animal. In this case a particular end organ sets up a series of nerve impulses which are average-frequency modulated in terms of intensity yet phase modulated in terms of input-signal phase. The transmission of a particular pulse across a synapse can be regarded as a most typical digital process yet the relative time of arrival gives a typical analog form of information. Perhaps I have thus destroyed your question instead of answering it.

Speed vs Equipment

E. Gruenberg: I would like to draw attention to the facts brought out here about the relatively slow speed of the individual operations of the brain, milliseconds as contrasted to the microseconds that we speak of in man-made machines. Of course, I should point out that the brain seems to beat out the man-made digital computer because of the fact that there are just so many operating centers. What I was wondering is, would anybody like to comment on what kind of machine design we could think of which would be more like the brain in this particular aspect, namely, slower in speed, but perhaps have more centers? I would think that it would be a little easier for human beings to do something with them because one wouldn't be outracing the other in some fantastic fashion as is done now.

N. Rochester: One thing is fairly clear, and that is that the brain has a lot of information available in its memory, a lot more than we put in the high-speed memories of our computers. It takes the brain longer to get this information out, but the brain has a wider choice. I can speak from hard experience about having a lot of information available; it really pays off! We, in the electronic computer business, have been trying to compete with other business machines. One clerk with a long array of punchcard files can very often beat out the best automatic computers!

I think this is related to the question you ask. Perhaps this is the direction we should go: to build larger scale memories with somewhat slower access speeds.

O. H. Schmitt: I don't think that there is anything intrinsically desirable about slow speed. We shouldn't object to operating neurons quickly if we could, but I think the emphasis here should be on the use of a different system which allows a large number of simultaneous cross-indexing searches to get to the dense center of information quickly, whatever the speed of access.

H. E. Tompkins: Let us not foreget that one can trade speed for equipment, and vice versa.

What Model Do We Want?

W. S. McCulloch: I would like to discuss a question which is always raised in my mind during such discussions as this. The question is, what kind of a model or theory does one want of the brain? If all one wants is a picture which preserves the logical relationships, then the picture is nothing but a row of buckets with pebbles in them to make it count. That is all the hardware he needs. But if he wants to carry over something which is a model in a mathematical sense, he has a far more complicated situation on his hands, and if he wants to know what particular chemicals are involved, and so on, particularly as a physician may want to know, or a pharmacologist may want to know, then he has got a still tougher job.

I am not quite sure what the questioner wants; that is, on what level he wants to place his question? Surely, the purely logical models in a logical sense are easily built.

H. E. Tompkins: Let us generalize a little bit and say that our question is a functional one as distinct from a logical model, because I think when you say a logical model you are assuming that the logic is the ordinary logic that we are familiar with.

A. G. Oettinger: The functional model can be com-

pletely adequate if we are interested in a machine duplicating a certain range of functions, but if your business is to understand the structure of the human brain as a human brain, then from there on I can't see how one can do this by any other means except to study the human brain itself. It strikes me that the issue is really what problem it is you are interested in. Are you interested in describing the human brain, or interested in formulating theories of brain-like functional behavior?

H. E. Tompkins: The question here is really, if you are after a machine, a functional description, to what extent does a study of the brain assist you? One might analogously ask, if one wants to design transistor circuits, to what extent should one study transistor physics as distinguished from external circuit properties? Can we narrow it to this question? To what extent, as computer engineers trying to build a machine which functions like the brain, can we benefit from a study of the neurophysiology of the brain?

The Neurophysiologists' Contribution

W. Pitts: I should like to discuss this question, and will divide the discussion up into three parts. Dr. Schmitt has already mentioned the strong points of the human brain, compared to the computer, namely, flexibility; capacity for dealing with a large quantity of data, selecting significant parts of it, throwing away the rest, and arriving at a roughly adequate decision; changing the whole method of behavior in case the general nature of experience changes; and making inductions. Whether it would be desirable to have a machine like that at all is the first question. If it were exactly like a man, it would cost far more than our man.

But are there not situations where we would like, so to speak, to have a man able to observe more things, to have more eyes, to keep his eyes wider open more of the time, to have more ears, more sense organs; in short, to take account of a much larger amount of simultaneous and successive incoming channels full of data, most of which are irrelevant, and on the basis of this, to discern whatever is significant for every purpose for which it is designed; and use those data to make decisions rapidly, improve the method of taking into account the data, and make decisions in view of the experience of success or failure. Well, I rather think there are such situations.

In the second case, let us suppose that it is desirable to have a machine which unites the advantages of having all of the input channels which one can build into a digital computer, but using the flexible rough logic of the brain. What is the best way of going about doing it? Well, Dr. Oettinger thinks what one ought to do is proceed by discovering exactly and with what principles the human brain learns and makes its inductions and makes its generalizations, and so on, and simply write that as a program for a suitable machine. This requires that we should have a complete psychology of learning in hand.

Of course, we don't have that. It is not a practical matter. Even then, the question of realization would perhaps be a serious one. Seeing that we have yet made no successful approach to what you might call a really scientific psychology of learning and concept formation and inductive reasoning, one might think that it is a sort of umpromising way of going about it. Perhaps we might be able to attack it by going the other way, by simulating the brain to some extent in the hope of finding, by trial and error, something that behaves similarly.

About the question of simulation: There are many differences between the brain and the computing machine that one would not want to eliminate in any new computing machine. In some respects that is certainly the case.

With respect to the parallel elements and reduplication, we don't know whether that really happens in the parts of the brain that actually do learning and generalization. I rather doubt it. I think that considerations of the total amount of memory, for example, would preclude it. It is obvious where one observes a track of, say, 1000 fibers leading to a single muscle, each contracting a single muscle fiber, producing different degrees of contraction; but that is an enormous waste of information, for you could code the hundreds of possible degrees of contractions in a few fibers. This reduplication happens mostly where the brain has to come into direct contact with a world composed of dynamic variables and behave accordingly, or again, where you have to translate a retina mosaic of intensity of light into one cortex. I think that it is not the case that *all* the memory and learning elements are reduplicated on this enormously vast scale.

Again, von Neumann's theory, in a sense, in the lower bound, is misleading. He proves only that if we reduplicate by so many channels, then you can improve the reliability by *at least* so much. He did not prove or attempt to prove that he could improve the reliability *only* so much.

Then, again, and perhaps more important, I should like to point out that in simulation, one does not have to attempt to simulate all of the structural detail. If one discovers that the functioning, say, of the retina, ending up in the cortex, is fundamentally simply to project the mosaic of the light on the retina into the brain, then one can certainly do that more cheaply in a machine by using a scanning mechanism and a small number of channels.

If one can divide the function of the human brain into blocks, and discover what each of these blocks does, then one can substitute for each of the blocks another device which is functionally equivalent, and which is more practical.

Finally, I would like to reduce the point to simple common sense. Supposing one is attempting to produce a new kind of machine to perform a function. Is it or is it not helpful to have at hand a model of the machine which one knows does perform that function, which model one only partially understands but which one

does partially understand, or is this of no value whatever? I should think from the point of view of common sense, it would be of value, particularly if one could not describe that function in a rigorous way.

A. G. Oettinger: I think the answer to it is probably "no," and the illustration that I gave of flight, I think, illustrates it rather well. The most obvious example of flight is the bird. For centuries men imitated birds by planning to fly with flapping wings, and fell on their heads. It was hard to realize there were other means available for flying which did not imitate the bird.

With regard to some of the other points, I think I have been used a bit as a straw man here, because I find myself in agreement, really, with most of what Dr. Pitts has said. My point of view, in brief, is this:

There are two problems. One is the design of machines to be used as tools to help us in performing certain functions. The other one is an attempt to understand the structure of the human brain. These two problems are not necessarily related.

Pattern Recognition

H. E. Tompkins: This might be a good time to have Mr. Rochester give a brief description of the recent experiment by Oliver Selfridge, which I believe has a bearing on this matter of a pattern recognition.

N. Rochester: I am sure I can't convey the meaning of it as well as Selfridge could, but unfortunately he wasn't able to be here. The problem which they have attacked is the problem of the operation of the retina, or perhaps of the function of the visual part of the brain.

They have gone after the problem of pattern recognition and , in particular, the problem of recognizing the letter "A." They start with a representation of an "A" as a set of ones and zeros, where the ones represent black and the zeros represent white, a rectangular array. Then they treat this array of information with an algorithm much as one would solve a partial differential equation. In fact, they have two algorithms. One smooths over small irregularities. It is believed that this happens in the retina. Another sharpens up the edges. By repeated applications of these two algorithms, processing the whole data, they find that they are able to take practically any "A" and reduce it to five spots, one at the vertex, two at each of the ends of the legs, and two at the places where the cross forms a junction with the sides.

In other words, they are able to take very irregular sorts of figures which we still recognize as A's and reduce them to these five spots in a pattern, which is a lot simpler. This looks like a fairly significant step toward forming an abstraction. In other words, you start with something very complicated, and end up with something quite a lot simpler, and it still contains the sa meinformation. Does that cover the point?

W. Pitts: Perhaps not as completely as one ought to altogether. What they are in essence doing is this. Let us suppose that one wants to make a machine that recognizes letters of the alphabet. Letters of the alphabet are alike, partly by simply being different in size; some are different in shape, but we have enough experience in different sorts of "A's," so that we call both the small printed "a" and the large capital printed "A" an "A," but they are only conventionally similar in shape.

We want to make a machine that does not simply read these, as if we put in a large catalog of all the possible styles of type which it compares with ad seriatem, but we want to make the machine learn to read, giving it a learning period in which it makes guesses and we tell it to print its guesses when its guesses are correct. If it is "A" and it happens to be "B" and we tell it it is a "B," and it is wrong, it changes it. What Selfridge does is have various fundamental operations that are performed on the figures such as averaging the edging, repeated edging that emphasizes corners, and some other complicated things which will not vary under rotation. The result, when he has applied a sequence of operations repeatedly on the figure, is a number.

Now, some of these numbers, if one computes them for various letters of the alphabet, are useful in distinguishing some letter from some other letters, but they will not distinguish certain letters from certain other letters. Other computed numbers will distinguish other letters from certain letters, but not distinguish them from the first, and it makes a random research of all, in the space of operators or functionals generated by taking perturbations of the fundamental operations, and applying a numerical operator at the end. So it performs a random search until it manages to find a collection of operation sequences that are able to distinguish all the letters of the alphabet, and it does this by experiment. It would work just as well with the Cyrillic alphabet.

H. E. Tompkins: Here is an excellent example of how an apparently simple problem is recognized as a major problem when one tries to reduce it to detailed terms, as Selfridge did. Recognizing the letter "A" seems to be child's play, and we teach children to do it, but it becomes a problem of substantial difficulty when we try to get a machine to solve it. Just what is the essence of "A" that permits us to recognize it so readily in spite of variations in its structures?

W. Pitts: Determining absolutely precise and exact rules for recognizing the letter "A," in all of the forms which ordinarily occur even in printed matter, would be an enormous job, if it were possible at all.

H. E. Tompkins: I would like to ask that any member of the audience who has a comment or question go to one of the aisle microphones.

Creative Thinking by Machines?

J. Rothstein: I have some general observations. First, though, let me say that I think I am on both sides of what a lot of the speakers said. This is a discussion on the whole business of analogy between the computer and the brain. On the one hand, people seem to realize that whatever one can specify operationally, one can, by the use of descriptive logical classifications and the iso-

morphism of logic and switching circuitry, set up a realization of it; one can realize a machine which will duplicate any operationally specified behavior. So in a sense, to construct an analog or simulator for a brain, all you have to do is to give an operational specification of what it is that you are trying to simulate.

Of course, that covers a multitude of sins, but even in that sense, you can say the problem is solved in principle. All you have to do is to go out and study and see what it is you are trying to imitate. I think that that misses the real problem by a great deal—which comes up when people say, "How can a machine create? What is the operation of creating?" There, people are usually stuck, because by its very nature creation seems to be not the sort of thing that one encounters when one simply scans over a known system. That is the sort of thing you get when you turn a crank. Wherein does the creation lie?

I think, perhaps, a clue might be found in the theorems of Goedel, who says, in effect, that in any logical system complicated enough to include something like arithmetic there are theorems which can be stated, but not proved or disproved in that system. But, when one proceeds to form an enlarged system, containing the first, one can very well have a new system in which the original question now has a perfectly well-defined answer.

There will be new questions in this new system that one can't answer. One cay say, perhaps, that creation consists in this act of enlargement and might even then say why it is as time goes on, if this be so, how progress is made. Because, you see, somehow or other a lot of what we see are first thought of as independent units, and then one can think of these as little logical systems, with creation involved in their fusion into a whole, an enlarged system. If one goes over the proof one suspects that many of these things (like creation) are essentially that sort of thimg—the things that one can't prove. We can't deny the power of creation to a machine until we can say what we are denying.

Another thing that was mentioned was this business about a machine being unable to make a decision on inadequate evidence. I think that this, too, is really in the nature of an issue that shouldn't be raised, because a decision theory is something that can be formalized, too, and if it can be, it can be built into a machine. So, for this reason, one doesn't advance the discussion by bringing this up in reference to a machine. And the same thing goes with reference to any sort of formalization of the process of induction, say if one bases it on decision theory or some equivalent theory.

Now, one more item, getting back to this creative business again: If one can make a model of anything whatsoever describable in logical terms and then build it into a machine, and so on, then one can really say that any field whatsoever that is communicable (inasmuch as one has to put things in terms of logical symbols and work in terms of definitions, whatever we say or talk about has to be put into buckets of this sort) can have an analog or simulator built for it. It reduces the whole problem to a triviality; but this doesn't go quite far enough.

Perhaps a little analogy might bring out the point here. Suppose one is interested, let us say, in the geometric properties of a sphere, and one has got used to dealing with a space of 24 dimensions. Well, one can clearly derive all the properties of a sphere in 3-space by discussing the geometry of a space of 24 dimensions, but this space is redundant as the dickens. As far as intrinsic properties of the sphere are concerned, 21 of the 24 dimensions are excess baggage.

Logic is such a broad sort of thing with regard to a discussion of this sort (and the specific disciplines and problems that we come up against have, so to speak, intrinsic properties of their own) that the real problem is not one of making an analogy, but of making an intrinsic analogy, so to speak.

This brings me, then, to my final observation. That is, when one wants to build a machine to be the analog of certain things, like brains, one can't argue from any analogy to the brain, because it may very well be that this analogy is highly redundant, in the above sense, and we may be arguing about properties that have no relation whatsoever to the brain's processes. But this doesn't mean that these analogies are useless. It may be possible by a consideration of the functions to be performed to find certain characteristics that all models must have in common. In other words, there may be some absolute requirements on the models, imposed by the behavior to be simulated, which will show up as common characteristics. If we discover such things, then I think we can argue, with perhaps some degree of confidence, that we have therefore found out something about the brain, too.

O. H. Schmitt: I believe I can fully justify the approach to computer engineering design via biological research in the following way: We know a great deal about the computer-like functions which a biological organism displays, and something about the mechanisms by which these results are achieved. We know that many of the biological techniques already known and constantly being discovered are quite different from the accepted engineering means for achieving similar ends. Where engineers have not tried out techniques analogous to the biological ones I say, "Look at them and try them out. If by chance they give answers, then analyze and adapt them for very likely they will lead to good answers and cheap answers." It is not safe or sensible to say offhand that the biological way is not a good way without adequate tests of each new case that arises, for it has so often led us to good solutions in the past.

H. E. Tompkins: There are many approaches yet to be made in this field, and I hope in this discussion today we have encouraged some of you to contribute your own bits to them, both in private and public discussions, to come.

Contributors

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From 1946 until August, 1956, he was with Bell Telephone Laboratories. While at the Laboratories he was first concerned with the design and development of mechanical and magnetic recording instruments and fundamental studies of magnetic recording. Following this he worked in the Switching Research Department on fundamental studies of digital storage devices, such as ferroelectrics and delay lines, and while engaged in this work pioneered in circuit applications of ferroelectrics. Since August, 1956, he has been with The National Cash Register Company as director of physical research.

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For a biography of Nelson T. Grisamore, see page 168 of the September, 1956, issue of IRE TRANSACTIONS ON ELECTRONIC COMPUTERS.

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Harold F. Heath, Jr. (A'52) was born October 13, 1923 in Peekskill, N. Y. He received the B.S degree in electrical engineering from Union College, Schenectady, N. Y. in 1951. He has since been engaged in computer development at the IBM Research and Development Center in Poughkeepsie, N. Y. His activities were primarily concerned with component engineering problems. Since 1955, he has been concerned with patent-engineering problems in the IBM Research Department.

Mr. Heath has been a member of several AIEE and RETMA committees on electronic components, particularly semiconductor devices. He is a member of Sigma Xi, Association for Computing Machinery, and the Operations Research Society of America.

❖

Robert M. Howe (M'54) was born in Oberlin, Ohio, on August 28, 1925. He received the B.S. degree in electrical engineering in 1945 from the California Institute of Technology, the A.B. in physics in 1947 from Oberlin College, the M.S. in physics in 1948 from the University of Michigan, and the Ph.D. in physics in 1950 from the Massachusetts Institute of Technology. From 1947 to 1948 he was a research associate at the Engineering Research Institute, University of Michigan, where he did basic research on the design and application of electronic analog computers. From 1949 to 1950 he carried on fundamental research in low-pressure mercury arcs as a research assistant at the Research Laboratory of Electronics, M.I.T.

In 1950 Dr. Howe returned to the University of Michigan in the Department of Aeronautical Engineering, where he is currently an associate professor, teaching courses in automatic control, guidance of pilotless aircraft and missiles, and nuclear engineering. In addition, he is continuing research on electronic differential analyzers and flight simulators.

Dr. Howe is a member of Phi Beta Kappa, Tau Beta Pi, Sigma Xi, the American Institute of Physics, and the American Association for the Advancement of Science.

❖

Velio A. Marsocci (S'50–A'55) was born on Long Island, N. Y., on June 7, 1928. From 1946 to 1949 he served as an electronic technician in the U. S. Navy. He received the B.E.E. degree in 1953 and the M.E.E. degree in 1955 from New York University. Mr. Marsocci served as a graduate assistant during 1953, and from 1954 to 1956 as an instructor in the electrical engineering department at New York University. He presently holds a position as assistant professor of electrical engineering at the Stevens Institute of Technology.

Mr. Marsocci is an associate member of the AIEE. He also holds membership in Tau Beta Pi and in Eta Kappa Nu.

❖

Richard E. Merwin (A'44–M'55) was born October 2, 1922 in East Palestine, Ohio. He graduated from the University of Pennsylvania in 1943 with the B.S. degree in electrical engineering. After working several months as a student engineer at the Allis Chalmers Manufacturing Co., he entered the U. S. Navy where he served two years as a Radar Maintenance Officer.

Mr. Merwin joined the research staff at the University of Pennsylvania in May, 1946, where he worked on the ENIAC and EDVAC projects. Three years later he joined the scientific staff of Los Alamos Scientific Laboratory to work on the MANIAC computer project. In May, 1951, Mr. Merwin went to work at the Poughkeepsie Laboratory of IBM where he has worked on computer projects including the 701, 702 and 705. He is currently a development engineer and manages a group re-

sponsible for the basic circuit design in the IBM Poughkeepsie Product Development Laboratory.

❖

Raymond E. Nienburg was born in Amityville, N. Y., on July 7, 1924. After spending three years in the U. S. Navy, he attended Massachusetts Institute of Technology, receiving the B.S. and M.S. degrees in electrical engineering in 1950. From 1949 to 1951 he was employed by the Cambridge Research Center and was involved in the early stages of the Lincoln project. In 1951, he accepted a position with the Research Laboratory at IBM in Poughkeepsie. In 1953, he became engaged in the design of the AN/FSQ-7 SAGE computer and has remained in computer development in the IBM Laboratory since that time.

Mr. Nienburg is a member of Eta Kappa Nu.

❖

Gregory J. Prom (S'52–A'53) was born in Harvey, N. D., on January 18, 1931. In 1952 he received the degree of Bachelor of Bachelor of Science in electrical engineering from North Dakota State College. Following this he took graduate courses in electrical engineering at the University of Minnesota part-time for two years.

From 1952 to 1955 he was employed as an electrical engineer by the Engineering Research Associates Division of Remington Rand, Inc., St. Paul, Minn. where he was engaged in the design and development of transistorized computer circuitry for a large scale digital computer. In 1955 Mr. Prom joined Sylvania Electric Products, Inc., Waltham, Mass., where he is a senior engineer in charge of a transistor group and is responsible for the design and development of transistorized digital switching circuits for computing and data processing equipment.

❖

Lawrence R. Walters (M'54) was born in New York, N. Y., on July 27, 1928. He received the degrees of B.E.E. and M.E.E. from Rensselaer Polytechnic Institute in 1949 and 1951. From 1949 to 1951, he taught Communication Engineering at Rensselaer. In June, 1951, he joined the IBM Poughkeepsie Development Engineering Laboratory. In 1953, he was assigned to Project High to develop maintenance programming and marginal checking for the AN/FSQ-7 air defense computer.

Mr. Walters is a member of Sigma Xi.

PGEC News

1957 Western Joint Computer Conference

The 1957 Western Joint Computer Conference, under the sponsorship of the IRE, American Institute of Electrical Engineers, and the Association for Computing Machinery, will be held in Los Angeles Calif., on February 26, 27, and 28, 1957. The conference theme, "Techniques for Reliability," is an extremely timely one. The conference will be organized with parallel sessions, one devoted to the conference theme and the other to outstanding papers of more general nature.

John L. Barnes, Systems Laboratories Corporation, is conference chairman; Gilbert W. King, International Telemeter Corporation, is publications chairman; William S. Speer, Norden-Ketay Corporation, is conference secretary; and Louis G. Walters, Aeronutronic Systems, Inc., is program chairman. Erwin Tomash, Telemeter Magnetics, Inc., has been appointed chairman of the Local Arrangements Committee with the subcommittee chairmen as follows: Exhibits, G. P. West, Ramo-Wooldridge Corporation; Hotel Arrangements, Jones Tupac, Rand Corporation; Printing, Ralph Singman, Sperry-Rand Corporation; Public Relations, S. D. Wanlass, Aeronutronic Systems, Inc.; Registration, A. C. Bellanca, Telemeter Magnetics, Inc.; Trips, Jack Donan, Clary Corporation.

Chapter Elections

The following chapters have reported on election of officers:

Baltimore
Chairman, Colin H. McAdie
Vice-Chairman, Martin Weik
Secretary, Sam Sternbach

Dallas-Fort Worth
Chairman, C. C. Calvin, Chance Vought
Vice-Chairman, R. L. Hines, Convair
Secretary, J. E. Howard, Chance Vought

Los Angeles
Chairman, Keitch W. Uncapher
Vice-Chairman, C. L. Wanlass
Secretary, J. Rosenberg

Dayton
Chairman, J. M. Mayer

New York
Chairman, W. S. Oliwa, Monroe Calculating Co.
Vice-Chairman, William Adler, W. L. Maxson Corp.
Secretary, M. J. Relis, Control Instrument Co.

Washington
Chairman, W. L. Anderson, Remington Rand

Chicago
Chairman, A. D. Aroem, Stewart-Warner Electronics

Chapter Meetings

Philadelphia
Robert Douthett, Sperry-Rand Corp., discussed developments on the LARC Computer at the October meeting.

Meetings

Dec. 10–12—IRE-AIEE-ACM Eastern Joint Computer Conference, Hotel New Yorker, New York, N. Y.

Jan. 14–15—Third National Symposium on Reliability and Quality Control in Electronics, sponsored by IRE, RETMA, and American Society for Quality Control, Hotel Statler, Washington, D. C.

Feb. 26–28—1957 Western Joint Computer Conference, Hotel Statler, Los Angeles, Calif.

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NOTICE—Readers who are mounting their reviews, and hence wish alter nate pages to be left blank are requested to write to the editor, J. P. Nash University of Illinois, Urbana, Ill., indicating their wish that this arrangemen be continued. Unless a number of readers request this, the blank pages wil be discontinued.—*The Editor*

Reviews of Current Literature

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NOTICE—Readers who are mounting their reviews, and hence wish alternate pages to be left blank are requested to write to the editor, J. P. Nash, University of Illinois, Urbana, Ill., indicating their wish that this arrangement be continued. Unless a number of readers request this, the blank pages will be discontinued.—*The Editor*

It is the intention of this section to review articles that have been published since January 1' 1953, and to publish eventually reviews of all books pertaining to the computer field. Authors can be of considerable assistance in this review process by sending two reprints of their articles to H. D. Huskey, Department of Electrical Engineering, University of California, Berkeley, California. The editors wish to express their gratitude to the reviewers who, through their efforts, make this section possible.—*H. D. Huskey*

GENERAL

56-150

Computers, Mathematics, Statistics, and Automation—Arthur Rose, R. Curtis Johnson, Richard L. Heiny, and Theodore Williams. (*Indus. Eng. Chem.*, vol. 48, pp. 622–632; 1956.) This paper is included in the fourth annual review of fundamentals of chemical engineering published each spring in Industrial and Engineering Chemistry. The authors attempt to give an exhaustive review of the year's literature pertaining to applications of computers, mathematics, and statistics in engineering chemistry. In addition, they discuss the current trends toward automation in chemical engineering in a way which provides a good background for chemical engineers interested in the subject. The present paper and its three predecessors in the series, 1) "Computers, Statistics, and Mathematics"—Arthur Rose, Joan A. Schilk, and R. Curtis Johnson, (*Indus. Eng. Chem.*, vol. 45, pp. 933–939; 1953); 2) "Computers, Statistics, and Mathematics"—Arthur Rose, Richard L. Heiny, R. Curtis Johnson, and Joan A. Schilk, (*Indus. Eng. Chem.*, vol. 46, pp. 916–922; 1954); 3) "Computers, Statistics, and Mathematics"—Arthur Rose, R. Curtis Johnson, and Richard L. Heiny, (*Ind. Eng. Chem.*, vol. 47, pp. 626–632; 1955), constitute a serious attempt to make available to chemists and other scientists and engineers the current status of applications of computers, mathematics, and statistics in the chemical industry.

C. B. Tompkins
Courtesy of *MTAC*

56-151

Automation—W. R. G. Baker. (1955 IRE Convention Record, part 4, pp. 54–57.) After brief comments on the difficulty of defining automation, the author points out that while common usage of the word "automation" is new, the phenomenon it describes has very few technical and no sociological elements that are new to this generation. In particular, he attacks those who claim that automation poses a threat to employment. Technical progress will always cause shifting of the working force to newer, previously undeveloped endeavors, but he points out that statistics have shown that the total number of jobs expands as our degree of mechanization increases.

J. D. Noe

56-152

Automation—R. W. Bolz. (1955 IRE Convention Record, part 4, pp. 58–59.) The author demonstrates his enthusiasm for automation and points to it as the only means to handle the disparity between extrapolated demands for manufactured goods, and the expected increase in our national working force. This is followed by a note on the concomitant need for more engineers with broad experience in many related fields.

J. D. Noe

681.142 56-153

Electronic Computers—(*Elektronische Rundschau*, vol. 9, October, 1955.) The main part of this issue is devoted to a series of papers on digital computers, with titles as follows:

Programme-Controlled Computers—H. J. Dreyer (pp. 341–343).

From the Punched-Card Computer to the EDPM [electronic data-processing machine]—O. Schröter (pp. 344–348).

Micro-program Control Mechanism—H. Billing and W. Hopmann (pp. 349–353).

The Parallel Adding Mechanism of the PERM [programm-gesteuerte elektronische Rechenanlage München]—W. E. Proebster (pp. 353–359).

Printing the Results from Electronic Computers—G. Overhoff (pp. 360–361).

Use of the Electronic Computer "GAMMA 3" for solving Complicated Mathematical Problems—H. Päsler (pp. 362–365).

Technical Problems in the Development of Magnetic-Drum Stores—H. O. Leilich (pp. 365–368).

Store Resonator Circuit and Data Input and Output for the Bull Electronic Computer "GAMMA 3"—R. Machery (pp. 369–370).

Assessment of Quality of Rectangular [-loop] Ferrites for Electronic Computers—O. Eckert, E. Weides, and K. Wallenfang (pp. 371–374).

Development of Resistances for Electronic Apparatus—H. Loth (pp. 375–376).

Transistors in Computer Technique—A. Krösa and K. Ganzhorn (pp. 377–380).

Properties required in Germanium Diodes for Electronic Computers—W. Bühler (pp. 381–382).

Courtesy of Proc. IRE
and *Wireless Engineer*

681.142:621.314.7 56-154

Transistor Circuits for Analog and Digital Systems—F. H. Blecher. (*Bell Syst. Tech. J.*, vol. 35, pp. 295–332; March, 1956.) A summing amplifier, an integrator, and a voltage comparator using junction transistors are described, together with a voltage encoder made up from them, for translating voltages into equivalent time intervals for analog-to-digital conversion.

Courtesy of Proc. IRE
and *Wireless Engineer*

621.372:621.314.7 56-155

Principles of Transistor Circuits—J. P. Vasseur. (*Ann. Radioélec.*, vol. 10, pp. 99–162; April, 1955.) A comprehensive review covering amplifiers, oscillators and flip-flops. Over 70 references.

Courtesy of Proc. IRE
and *Wireless Engineer*

621.314.7:621.385 56-156

Transistors versus Vacuum Tubes—D. G. Fink. (Proc. IRE, vol. 44, pp. 479 482; April, 1956.) The relative merits of these two types of device are compared with reference to particular applications; possible future developments are briefly indicated.

Courtesy of Proc. IRE
and *Wireless Engineer*

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—*The Editor*

621-52:681.142 56-157

Digital Methods in Control Systems—D. F. Nettell. (*Electronic Eng.*, vol. 28, pp. 108–114; March, 1956.) The application of digital computer techniques to factor automation is discussed, with special reference to the use of digital methods with existing analog installations.

Courtesy of PROC. IRE and *Wireless Engineer*

56-158

Analog-to-Digital Conversion—M. L. Klein, F. K. Williams, and H. C. Morgan. (*Instruments and Automation*, vol. 29, pp. 911–917; May, 1956.) The three basic techniques of analog-to-digital conversion are discussed. These are time encoding, feedback encoding or voltage-comparison, and space encoding. Requirements on conversion rates, accuracy, time to complete one conversion, and ambiguity are well presented. Each of the basic techniques is described and examples of typical circuits are given. Practical limitations on capacity, operating speeds, and accuracy of each basic converter are considered. Advantages and disadvantages of different types of encoders are stated. The feedback encoding is the least developed of the three but offers a good deal of promise. The survey is comprehensive enough to bring the reader up-to-date in this field.

Raymond Davis

56-159

Practical Analog-Digital Converters—M. L. Klein, F. K. Williams, and H. C. Morgan. (*Instruments and Automation*, vol. 29, pp. 1109–1117; June, 1956.) The previous paper in the May issue (see pp. 56–158) described the three basic techniques of analog-digital conversion. This paper is a survey of the commercial converters manufactured by various concerns. The converters are classified in terms of function and mechanism. These are space encoders with coded discs and brushes, space encoders with coded discs and phototubes, space encoders with inductive or magnetic elements, space encoders with D'Arsonval movement, space encoder for tank gaging, shaft quantizers for digital printout or readout, all-electronic data loggers and all-electronic high-speed converters. A brief description with an illustration of commercial converters in each category is given. The paper will be useful to the reader who has an analog-digital conversion application.

Raymond Davis

56-160

Electronic Computers and Personnel Administration—Lowell H. Hattery. (*Personnel Administration*, vol. 19, pp. 7–13; March–April, 1956.) The often-ignored problem of personnel relations in the installing of electronic data processing systems is given a lucid and practical treatment. Not only are the problems presented, but concrete suggestions given for immediate steps toward their solution. Although the article is concerned with government installations and Civil Service personnel, the points made are equally valuable to business mangaement. The problems presented, along with their solutions are the following: 1) Fear of displacement, resulting in lowered morale and hasty resignation by all levels of personnel who are affected in some way by the new equipment. Solution: The Pacific Mutual Insurance Company program of employee relations is given as an outstanding example of eliminating this problem before it arises. 2) Lack of job evaluation, qualifications, standards. Solution: It is suggested that the Civil Service Commission in particular, and business management in general, speedily set up a program of study, and recommend basic policies in these areas. 3) Inadequate training programs for all levels of personnel, including long-range career planning. Solution: Training for the individuals affected by the system should be increasingly the task of the employer, and the universities. An important aspect is the stimulation of employees and others to view business electronics as a career. In all these solutions, "the personnel officer has a responsibility to cooperate with other management officers toward a program to reassure affected personnel, and, more important, to motivate all involved to contribute positively to the success of the new system."

Margaret Milligan

56-161

Simulation by Modeling—N. L. Irvine and L. Davis. (*Proc. Western Joint Computer Conf., Los Angeles, Calif.*, pp. 13–16; March 1–3, 1955.) The authors classify simulation-by-modeling into three categories, 1) analog models which obey the same laws as the phenomena under study, 2) mathematical models which describe the phenomena and need computation for their interpretation, and 3) scaled models of equipment subjected to actual or simulated environments. The authors are concerned primarily with the design of multidimensional (space) filters, which they show can be studied through simulation by modeling. The paper points out that space filtering may be extended to n dimensions, and to include color, intensity, location, and geometric shape. The detection of an electrical signal in the presence of noise is cited as an example, when the configuration of the noise-removing filter matches the desired signal, a high degree of transmission is obtained compared with that from a nonmatching condition. As a particular example of a system to be simulated, the paper describes an optical-electrical-mechanical model for detecting a round source of radiation immersed in a general distribution of unwanted radiation, such as a clouded sky. The model is an optical system composed of a light source, a holder to position photographs of the round source in any one of many possible background distributions, a fixture to mount a rotatable optical filter of appropriate weighting function for scanning the transmitted light, and a lens system to image the photograph and the filter onto a recording photometer. The authors demonstrate mathematically that such a model can be used to design an optimum space filter without recourse to the enormous amount of computation which would otherwise be entailed in evaluating the corresponding n-dimentional transforms. The paper provides an excellent presentation of the usefulness of simulation by modeling, and it is recommended reading for all engineers who may be helped by this kind of simulation.

Morris Rubinoff

ANALOG COMPONENT RESEARCH

56-162

Analogue Multiplying Circuits Using Switching Transistors—K. Chen and R. O. Decker. (1956 IRE CONVENTION RECORD, Part 4, pp. 74–80.) All-electronic transistor circuits of rather high speed are described. Techniques involve variation of width, amplitude, and repetition rate of pulses. Simplicity and ruggedness of equipment can be expected, together with advantages in size, weight, and power requirements. A four-quadrant laboratory model of function multiplier uses four transistors and is claimed to have errors less than 1 per cent of full scale. It requires an external triangular wave generator. A two-quadrant multiplier with errors under 2 per cent uses six transistors. Each input variable can vary over a range of at least 10:1 at present. The stated response time of 1 millisecond is fairly meaningless without a definition of the dynamic error. The product voltage is a train of pulses which requires smoothing by external circuits. The claim of "simplicity" less than an arbitrary equivalent of 6 vacuum tubes excludes consideration of input and driving requirements and auxiliary generators. Good temperature stability is claimed, and unstabilized power supplies are stated to be adequate, but no quantitative statement is included. The reader may experience some confusion in the "inverted" connection terminology. This is an interesting development of real potential value, especially in special purpose analog equipment.

Howard Wright

56-163

Analog Multipliers and Squarers Using a Multigrid Modulator—R. L. Sydnor, T. R. O'Meara, and J. Strathman. (IRE TRANS., vol. EC-5, pp. 82–85; June, 1956.) This article describes the use of a multigrid vacuum tube as an AM multigrid modulator multiplier. The accuracy of the multiplier is dependent only upon the linear properties of the vacuum tube used and not upon careful adjustment of the operating potentials. It is unusual that such a simple device should give a range of 78 db with only a ± 2 per cent full scale error. The advantages and also restrictions of this device along with a complete range of dynamic performance are included in this article.

Courtesy of PROC. IRE

681.142:621.37 56-164

An A.M.-A.M. Multiplier—L. Lukaszewicz. (*Bull. Acad. Polon. Sci., Classe* 4, vol. 3, pp. 145–148; 1955. In English.) A relatively simple purely electronic multiplier circuit for differential analyzers is described. Working with an upper frequency limit of 10 kc for both factors, accuracy is within about 0.3 per cent of full scale.

Courtesy of PROC. IRE and *Wireless Engineer*

681.142 56-165

An Electronic Generator for Functions of Two Independent Variables—V. Wentzel. (*Ericsson Tech.*, vol. 11, pp. 183–225; 1955.) A unit built at the Chalmers University of Technology is described. The function is recorded on a photographic plate in the form

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of variable-width columns; these are scanned by a cr tube. The output is either in the form of width-modulated pulses or in the form of a voltage proportional to the function.

Courtesy of PROC. IRE and *Wireless Engineer*

681.142 56-166

Function Generators based on Linear Interpolation with Applications to Analogue Computing—E. G. C. Burt and O. H. Lange. (*Proc. IEE*, part C, vol. 103, pp. 51–58; March, 1956.) By using suitable combinations of diode circuits and high-gain feedback amplifiers, it is possible to generate functions without restriction to monotonic characteristics. Experimental results are presented for a sin x generator in which the error is about $\frac{1}{2}$ per cent of the maximum output.

Courtesy of PROC. IRE and *Wireless Engineer*

56-167

An Electronic Circuit for the Generation of Functions of Several Variables—Hans F. Meissinger. (1955 IRE CONVENTION RECORD, Part 4, pp. 150–161.) Arbitrary functions of two or more variables can be generated by the use of biased diode ("ladder network") function generators. A second variable is applied in the form of the voltage applied to the bias-setting voltage divider, or, in more complicated cases, to the individual diodes through other function generators. The article contains an excellent summary with practical suggestions for dealing with the synthesis of such a function generator in the more complicated cases. For example one can handle certain intersecting or nonmonotonic families of curves (though the latter does not imply an ability to produce a negative resistance with diode networks). Classes of functions are tabulated indicating the probable complexity of equipment.

R. Stuart Mackay

ANALOG EQUIPMENT

56-168

A Practical Approach to Analog Computers—John D. Strong. (*The Computer Handbook*, edited by Milton H. Aronson, The Instruments Publishing Co., Pittsburgh, Pa., pp. 18–26; 1955.) The author briefly describes the basic elements of electronic analog computers and their modes of operation, with particular reference to practical details of the Electronic Associates' Model 16-31R. The stated purpose of the article is to show the "average engineer who has some electrical experience" how the computer solves problems. Most of the discussion is concerned with attenuators (including loading effects), inverters, summers, integrators, servo-multipliers and the control panel. Just mentioned in passing are arbitrary function generators and resolvers. The article is copiously illustrated with computer photographs and with schematics for various computer operations. Illustrative problems include polynomial equation solving, falling body, and vibrating mass. Scale factors are discussed. A brief comment is given on the oft-recurring theme "Analog vs Digital."

Walter W. Soroka

681.142 56-169

The Short Electronic Analogue Computer—R. J. A. Paul. (*Overseas Engr.*, vol. 29, pp. 205–208; January, and pp. 251–252; February, 1956.) Description of the design and operation of a general-purpose computer designed for quantity production and capable of single-shot and repetitive operation.

Courtesy of PROC. IRE and *Wireless Engineer*

621.317.729 56-170

An Electrolytic-Tank Equipment for the Determination of Electron Trajectories, Potential and Gradient—D. L. Hollway. (*Proc. IEE*, Part B, vol. 103, pp. 155–160; March, 1956. Discussion, pp. 163–165.) A description is given of equipment for testing either axially symmetric or two-dimensional systems; it can be switched to measure potentials, to mark equipotentials automatically, to measure potential gradients, and to trace electron trajectories. The accuracy is sufficient for most problems of electrode design.

Courtesy of PROC. IRE and *Wireless Engineer*

681.142:621.3:620.16 56-171

Shock Spectrum Computer for Frequencies up to 2000 c/s—C. T. Morrow and D. E. Riesen. (*J. Acoust. Soc. Amer.*, vol. 28, pp. 93–101; January, 1956.) An arrangement for investigating the effects of mechanical shock on electronic equipment installed, *e.g.*, in guided missiles comprises an analog computer which operates on an accelerometer signal, either direct or recorded, and solves the differential equation for the part involved, the result being displayed on a cro screen. The computer can be tuned up to 2 kc thus covering the range within which the fundamental resonance of any delicate structure is likely to occur.

Courtesy of PROC. IRE and *Wireless Engineer*

UTILIZATION OF ANALOG EQUIPMENT

681.142 56-172

Construction and Method of Operation of Modern Integrating Equipment [differential analysers]—H. Hoffmann. (*Elektrotech. Z. Edn A*, vol. 77, pp. 41–52; January 11, and pp. 77–83; February, 1956.) General principles are discussed and a detailed description is given of an installation in Germany. The results are presented to three or four significant figures by counter mechanisms, and in the form of curves on function benches. Curves of empirical functions are dealt with by photoelectric scanning. Errors do not exceed 0.1 per cent –1 per cent.

Courtesy of PROC. IRE and *Wireless Engineer*

56-173

The Effect of Bandpass Limitations on Analog Computer Solutions—J. Kaiser, Jr. and E. J. McGlinn. (*Industrial Math.*, vol. 6, pp. 7–15; 1955.) The authors point out that certain limitations are imposed on analog computer solutions of equations of the form $\ddot{y}+2rw\dot{y}+w^2y=F(t)$. These limitations are due primarily to band-pass characteristics of the computer components, in particular of amplifiers and integrators. Errors caused by such band-pass limitations can be estimated from graphs given in this paper. It is shown that errors introduced can cause a theoretically stable loop to become unstable.

S. D. Conte

56-174

Transfer-Function Synthesis with Computer Amplifiers and Passive Networks—M. V. Mathews and W. W. Seifert. (*Proc. Western Joint Computer Conf., Los Angeles, Calif.*, pp. 7–12; March 1–3, 1955.) This paper describes three systematic methods for the synthesis of complex transfer functions by the use of operational amplifiers with the appropriate input and feedback networks. First, the well-known method which employs one amplifier with the associated two-terminal feedback and input networks is presented in general form; this method is further expanded to include the use of three terminal networks. The second method is an original three-amplifier design with associated RC networks by means of which, it is claimed, any transfer function can be realized. The third method mentioned uses integrators to synthesize the polynomials of the transfer functions. An illustrative example for the first two methods is given in the paper and the circuits are constructed which allow a comparison between the theoretical results and the one amplifier and the three amplifier realization of the synthesis.

Cyril P. Atkinson

56-175

Delay-Line Method for Compensating Closed-Loop Systems in the Time Domain—Yu-Chi Ho and Ronald E. Scott. (1955 IRE CONVENTION RECORD, Part 4, pp. 24–36.) A delay-line method is presented for compensating a closed-loop system. The method is based on the reshaping of the open-loop impulse response of the system, from which one proceeds to calculate the closed-loop step response of the system. The method is the time domain parallel of the frequency domain method for closed-loop system synthesis. It is suggested that both methods be used to give a better physical picture of the compensation process. An hypothetical motor is used as an example of a discrete filter compensation design. An electronic analog computer is used to simulate the example. Also a four-stage ladder network is used to approximate the delay operator e^{-st} in an attempt to compensate a servomultiplier.

Cyril P. Atkinson

56-176

Electrical Analogues for Heat Exchangers—R. L. Ford. (*Proc. IEE*, Part B, vol. 103, pp. 65–82; January, 1956.) Author's summary: The paper is concerned with the derivation of dynamically accurate electrical analogs for heat exchangers with a view to their application in the solution of automatic-control problems relating to the latter. The analogs are based on idealized equations describing the behavior of the thermal processes involved. Two heat exchangers, both distributed-parameter systems, are considered, and two analogs are derived for each. One type of analog is composed almost entirely of passvie components but the other contains electronic amplifiers and employs a feedback technique. The design and con-

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ction of a passive-network analog is de-
bed, and its experimentally-determined
uency responses are given and compared
n the theoretical responses of the heat ex-
nger. Finally, an example is given of the
erimental application of the analog in an
omatic-control loop.

D. E. Hart

DIGITAL COMPONENT RESEARCH

.318.5:312.62:681.142 56-177

**The Cryotron—a Superconductive Com-
er Component**—D. A. Buck. (Proc. IRE,
. 44, pp. 482–493; April, 1956.) "The
dy of nonlinearities in nature suitable for
nputer use has led to the cryotron, a de-
e based on the destruction of supercon-
ctivity by a magnetic field. The cryotron,
its simplest form, consists of a straight
ce of wire about one inch long with a sin-
layer control winding wound over it.
rrent in the control winding creates a
gnetic field which causes the central wire
change from its superconducting state to
normal state. The device has current
n, that is, a small current can control a
ger current; it has power gain so that
otrons can be interconnected in logical
works as active elements. The device is
o small, light, easily fabricated, and dis-
ates very little power."

Courtesy of Proc. IRE
and *Wireless Engineer*

56-178

**A One-Microsecond Adder Using One-
gacycle Circuitry**—A. Weinberger and
L. Smith. (IRE Trans., vol. EC-5, pp.
-73; June, 1956.) An analysis of the func-
nal representation of the carry digits in
addition process shows that the one-
gacycle circuitry of SEAC and DYSEAC
be organized logically to permit the for-
tion of many successive carries simultane-
ly. The Boolean expression for any carry
it C_k can be expanded so as to be an ex-
it function of only the input digits of or-
s k to $k-p+1$ and of the carry digit
$_p$. Certain factorizations can then be
de to simplify these expressions so that all
them fall within the limitations on the
ing complexity imposed by the circuitry.
arallel adder utilizing this principle is de-
oped which is capable of adding two 53-
numbers in one microsecond, with rela-
ely few additional components over those
uired in a parallel adder of more conven-
nal design.

Courtesy of Proc. IRE

.385.832 56-179

**Deposition and Removal of Electric
arges on Insulators by Secondary Emis-
n: Part 1**—M. Barbier. (*Ann. Radio-
t.*, vol. 10, pp. 182–214; April, 1955.) A
ailed theoretical study is presented of the
cesses involved in recording signals in the
n of charges on insulator plates in cath-
-ray tubes; the field distributions and
ondary-electron paths are analyzed for
ne simple configurations. Possible accu-
lations of space charge are taken into ac-
nt, and estimates are made of the amount
harge that can be deposited, the limits of
resolution to be expected, the accumulation factor, and the beam intensity required for writing or reading.

Courtesy of Proc. IRE
and *Wireless Engineer*

56-180

Digital Storage Using Neon Tubes—M. S. Raphael and A. S. Robinson. (*Electronics*, vol. 29, pp. 162–165; July, 1956.) The digital storage device described uses the presence or absence of NE-2 neon tubes as the memory element. The information content of the memory matrix is fixed for a particular arrangement of neon tubes within the matrix. The neon tubes are arranged much as cores are in a core matrix, that is, at the intersection of a pair of matrix wires. In order to interrogate a memory position one half the NE-2 firing voltage is applied to one vertical and one horizontal matrix wire. The only neon to fire is one located at the intersection of the selected wires, if present, since only this location has the full firing voltage applied. The neons are contained with a photomultiplier tube in a light tight enclosure. The phototube will pick up the light output from any neon, thereby acting like a logical or gate and producing an output when any neon is fired. Since neon tubes are more difficult to fire when in total darkness, a flasher lamp provides the necessary excitation during interrogation. Signals from the phototube are inspected after the flasher lamp has extinguished. The memory described contained 256 bits and operated at a required read out rate of 200 cycles per second although operation at 2 kc was attained. The additional circuits required for cycling through all 256 bits were also described.

Norman F. Lorenz

621.318.57:621.374.3:621.387 56-181

Batching and Counting using Gas-Filled Decade Tubes—W. Grimmond and W. H. P. Leslie. (*Electronic Eng.*, vol. 28, pp. 138–143; April, 1956.) A range of units is described from which a variety of frequency meters, batching counters, etc., can be quickly assembled; circuit diagrams are given.

Courtesy of Proc. IRE
and *Wireless Engineer*

538.221:621.318.1 56-182

Ferromagnetism in Relation to Engineering Magnetic Materials—F. Brailsford. (*Proc. IEE*, part A, vol. 103, pp. 39–51; February, 1956.) " . . . a review is given of theoretical and experimental work mainly within the past ten years. This includes an account of ferromagnetic domains and of the small-particle theory of high coercivity. A description of the ferrites and of ferrimagnetism is given, and this is followed by a discussion of recent observations and ideas on the magnetic phenomena occurring at frequencies up into the microwave region."

Courtesy of Proc. IRE
and *Wireless Engineer*

56-183

Dynamax—A New Crystal and Domain-Oriented Magnetic Core Material—G. H. Howe. (*Electrical Eng.*, vol. 75, pp. 702–704; August, 1956.) This article describes experimental work and metallurgical development carried out in the development of a new high-permeability magnetic material named Dynamax. This material consists of 65 Permalloy with 2 per cent molybdenum added. The dynamic and static characteristics of toroidal cores built from thin tapes are described, showing some of the effects of annealing temperature, cold working, and tape thicknesses. One sample exhibits $B_s = 12{,}640$, $B_r = 11{,}940$, $H_c = 0.0055$, $\mu(\max) = 1{,}530{,}000$. Tape thicknesses in the range 2–10 mils are used here, and dynamic hysteresis loops are taken at 60 cps and 400 cps.

H. T. Larson

56-184

Bimag Circuits for Digital Data-Processing Systems—William Miehle, John Paivinen, and Joseph Wylen. (1955 IRE Convention Record, Part 4, pp. 70–83.) This article describes how magnetic cores with rectangular hysteresis loops can be used to store and manipulate digital information. The circuits are basically derived from two-cores per-bit magnetic shift registers. Novel features of those circuits include the use of split-winding loops and inhibit-transfer loops. In those loops, two diodes are used. The operation depends on the fact that a magnetic core presents a high inductance only when it changes its polarity of saturation. Diagrams are given to show how to achieve the functions of *or*, *inhibit*, *and*, *exclusive-or*, *negation*, and serial and parallel shift register. In all circuits, two or more phases of clock pulses are required. This article has been reproduced in substantially the same form in the Proc. IRE, vol. 44, pp. 154–162; February, 1956, and in the April May, 1956, issue of *Automatic Control*.

Way Dong Woo

681.142:162.314.7 56-185

Discussion on "A Transistor Digital Fast Multiplier with Magnetostrictive Storage," Before the Radio and Telecommunication Section, 9th November, 1955—(*Proc. IEE*, Part B, vol. 103, pp. 121–124; March, 1956.) This is a discussion of a paper by G. B. B. Chaplin, R. E. Hayes, and A. R. Owens which appeared in the same journal, part B, vol. 102, p. 412; July, 1955 (Paper No. 1858R). The discussion centers around the use of point-contact transistors, the use of transistors and tubes in combination, the use of base coils, and the delay line store.

D. E. Hart

621.314.7 56-186

Factors affecting Reliability of Alloy Junction Transistors—A. J. Wahl and J. J. Kleimack. (Proc. IRE, vol. 44, pp. 494–502; April, 1956.) Report of an investigation of the effects on Ge *p-n-p*-transistors alloyed with In and *n-p-n*-transistors alloyed with As-doped Pb of exposure to oxygen, water vapor and other gases. Changes of the breakdown voltage, reverse current, and current gain are produced by oxygen and water vapor in opposite senses; no observable changes were produced by pure hydrogen, nitrogen or helium. The changes produced are reversible; the true characteristic can be restored by baking in vacuum at a suitable temperature. Very high stability of characteristics can be achieved if water vapor and oxygen are completely excluded in this way.

Courtesy of Proc. IRE
and *Wireless Engineer*

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—The Editor

621.314.7 56-187

Diffused Emitter and Base Silicon Transistors—M. Tanenbaum and D. E. Thomas. (*Bell Syst. Tech. J.*, vol. 35, pp. 1–22; January, 1956.) Techniques are described for making Si *n-p-n* transistors by diffusing impurities from the vapor phase. Base layers 3.8×10^{-4} cm thick have been produced. Characteristics are presented of a transistor for which $a_0=0.97$ and cutoff frequency is 120 mc. The structure and design of these transistors are discussed. For a brief version see *Electronics*, vol. 29, pp. 137–139; February, 1956 (Carroll).

Courtesy of PROC. IRE and *Wireless Engineer*

621.314.7 56-188

A High-Frequency Diffused-Base Germanium Transistor—C. A. Lee. (*Bell Syst. Tech. J.*, vol. 35, pp. 23–34; January, 1956.) Techniques of impurity diffusion and alloying in Ge are discussed. Examples are given of Ge *n-p-n* junction transistors in which $a_0=0.98$ and cutoff frequency is 500 mc. For a brief version see *Electronics*, vol. 29, pp. 137–139; February, 1956 (Carroll).

Courtesy of PROC. IRE and *Wireless Engineer*

56-189

Surface-Barrier Transistor Switching Circuits—Ralph H. Beter, William E. Bradley, Ralph B. Brown, and Morris Rubinoff. (1955 IRE CONVENTION RECORD, Part 4, pp. 139–145.) This introductory discussion of direct-coupled transistor circuits should be of interest to both computer circuit engineers and logical designers. The characteristics of surface-barrier transistors which make direct-coupled saturating amplifiers possible are presented. Combinations of these amplifiers to produce flip-flops, monostable multivibrators, and gating circuits are discussed with particular emphasis on flip-flop and gating circuits. Design techniques are superficially treated and the fascinating possibilities of direct-coupled logic are only hinted at; however, the paper should prove valuable as an introduction to this new and important technique.

Dale Scarbrough

56-190

A Junction-Transistor Scaling Circuit with 2 Microsec Resolution—G. B. B. Chaplin and A. R. Owens. (*Proc. IEE*, Part B, vol. 103, pp. 510–515; July, 1956.) Author's summary: When junction transistors are used in conventional scaling circuits the maximum speed of operation is limited by the associated circuit, mainly owing to the use of capacitors, which require time to charge and discharge. The limiting speed of a transistor itself, which depends on the switch-on and switch-off times of current, is generally several times higher than this, but cannot be taken advantage of owing to the associated circuit. The basic binary scaling circuit described in the paper overcomes this difficulty by dispensing with capacitors, a differentiating transformer being used instead for coupling. In this way the speed of the circuit depends only on transistor characteristics. With currently available low-frequency junction transistors ($f_{cod}\cong500$ kc) the circuit is capable of reliably resolving 2 microsec. The basic binary scaler is readily adapted to the formation of a scale-of-5 circuit using three binary stages. When this is preceded by another binary scaler, the result is a scale-of-10 circuit with the same resolving capabilities as the original binary circuit. The circuits have wide tolerances and are insensitive to transistor variations. A complete scale-of-10 circuit uses eight transistors, ten diodes, and five transformers.

D. E. Hart

56-191

A Point-Contact Transistor Scaling Circuit with 0.4 Microsec Resolution—G. B. B. Chaplin. (*Proc. IEE*, Part B, vol. 103, pp. 505–509; July, 1956.) Author's summary: There is a wide choice of scaling devices which will operate at maximum counting rates up to several hundred kilocycles per second, but for counting rates in the region of megacycles per second, the choice is limited almost entirely to special thermionic scaling devices or circuits using thermionic valves. Such circuits tend to be rather complex and have a relatively high power consumption. The paper describes some scaling circuits using transistors which will resolve 0.4 microsec and hence count at a maximum rate of 2.5 mc. The transistors are the normal point-contact type, and the circuits are simple, they have wide tolerances and are economical in power consumption. Features which contribute to the short resolving time are the prevention of bottoming of collector potential and the absence of capacitors. A typical scale-of-10 circuit uses seven transistors, seven pulse transformers, and 14 crystal diodes.

D. E. Hart

537.227:.228 56-192

Electrostriction—H. F. Kay. (*Rep. Progr. Phys.*, vol. 18, pp. 230–250; 1955.) A survey paper. Ferroelectric materials are discussed with particular emphasis on the ceramic-oxide group, in which striction coefficients can be obtained which are high compared with those of true piezoelectric materials having irreversible polarity. There is still considerable doubt as to the exact mechanisms involved. About 50 references.

Courtesy of PROC. IRE and *Wireless Engineer*

537.227 56-193

Properties of Guanidine Aluminum Sulfate Hexahydrate and some of its Isomorphs—A. N. Holden, W. J. Merz, J. P. Remeika, and B. T. Matthias. (*Phys. Rev.*, vol. 101, pp. 962–966; February 1, 1956.) Report of an experimental study of this new class of ferroelectrics. The crystals are trigonal, with the ferroelectric direction along the trigonal axis. The 60 cps hysteresis loops are often biased or double, the shape being correlated with the location of the specimen in the mother crystal. At room temperature the saturation polarization is about 0.35 $\mu C/cm^2$ and the coercive force at 60 cps in 1–3 kv/cm; these quantities increase with falling temperature. The small-signal dielectric constant is about 6 along the axis and about 5 perpendicular to it. The switching characteristics resemble those of $BaTiO_3$, but the present crystals are considerably slower.

Courtesy of PROC. IRE and *Wireless Engineer*

537.226/.227:[546.48+546.33].882.5 56-194

Solid Solution Effects, Structural Transitions and Ferroelectricity in Sodium-Cadmium Niobates—B. Lewis and E. A. D. White. (*Acta Cryst.*, vol. 8, part 12, p. 849; December 10, 1955.) Results of a detailed experimental investigation of $NaNbO_3$-$Cd_2Nb_2O_7$ ceramics indicate that at any temperature the local Cd concentration within each crystallite determines whether the structure is ferroelectric or antiferroelectric. Macroscopically, the ratio of the two modifications depends on the over-all Cd concentration and on the temperature.

Courtesy of PROC. IRE and *Wireless Engineer*

537.226/.227:546.431.824-31 56-195

Dependence of the Coercive Force and Permittivity of Ceramic Barium Titanate on Mechanical Strains—N. A. Roi. (*Akust. Zh.*, vol. 1, pp. 352–355; October/December, 1955.) Experimental results indicate that the coercivity can be increased by means of mechanical tension. The form of the permittivity/temperature curves cannot be explained on the basis of a simple thermodynamic theory neglecting the effects of changes in the domain structure.

Courtesy of PROC. IRE and *Wireless Engineer*

537.226/.227:546.41/.431.824-31 56-196

Structural Behaviour in the System (Ba, Ca, Sr) TiO_3 and its Relation to Certain Dielectric Characteristics—M. McQuarrie. (*J. Amer. Ceram. Soc.*, vol. 38, pp. 444–449; December, 1955.) For compositions near the solubility limits in the ternary system (Ba, Ca, Sr) TiO_3 firing temperature has a marked effect on dielectric properties. No evidence of ferroelectric properties was discovered in $CaTiO_3$-$SrTiO_3$ systems.

Courtesy of PROC. IRE and *Wireless Engineer*

537.226/.228.1:546.431.824-31 56-197

Electromechanical Properties of Barium Titanate Ceramics—G. Mesnard and L. Eyraud. (*J. Phys. Radium*, vol. 16, pp. 926–938; December, 1955.) The elastic, electrostrictive, and dielectric properties of $BaTiO_3$ ceramics have been investigated by a resonance method, using disk specimens with their faces silvered to form capacitors; the equivalent circuit is derived, also the Q factor and the coefficient of electromechanical coupling for static fields up to 20 v/cm and for the temperature range from −150° to +150°C.

Courtesy of PROC. IRE and *Wireless Engineer*

DIGITAL SYSTEMS RESEARCH

681.142:621.314.7 56-198

Transistor Digital Computers—(*Wireless World*, vol. 62, pp. 210–212; May, 1956.) A brief account is given of circuit techniques involving the use of transistors and ferrite two-state storage devices described at the *IEE* convention on digital computers held in London in April, 1956.

Courtesy of PROC. IRE and *Wireless Engineer*

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—The Editor

56-199

A Servo System for Digital Data Transmission—R. H. Barker. (*Proc. IEE*, Part B, vol. 103, pp. 52–64; January, 1956.) Author's summary: Certain special features must be taken into account in the design of a servosystem which is to operate satisfactorily with digital data. In particular, the data are quantized in amplitude, thereby introducing nonlinear effects; they constitute a series of samples instead of a continuous function, and there may be significant delays due to low-speed transmission circuits or digital equipment or both. All of these contribute in various ways towards reducing the stability of the system. The method of synthesis takes full account of the sampling and delay features and enables a degree of prediction to be incorporated which ensures that the regenerated data do not lag on the original under steady-state conditions. Effects especially attributable to amplitude quantization are then studied qualitatively. Since stability diminishes and the sensitivity to noise and instrumental errors increases as the time of prediction is increased, it is essential that the delay involved in the transmission of each sample should be minimized. Furthermore, the sampling servosystem is less efficient than a continuous one as a smoothing device, and as much smoothing as possible should be applied at the sending end before sampling.

D. E. Hart

56-200

A Theorem on SPDT Switching Circuits—B. D. Rudin. (*Proc. Western Joint Computer Conf., Los Angeles, Calif.*, pp. 129–132; March 1–3, 1955.) The author apparently is attempting to develop an analytical approach to the design of switching networks where the SPDT switch is to serve as the basic element. Two wiring rules are suggested but the real significance of the article eludes the reviewer. The author indicates at the conclusion of the paper considerable apprehension over the possibility that the presentation may have been too brief. The reviewer feels his concern is certainly justified.

A. S. Hoagland

DIGITAL EQUIPMENT

56-201

The Wisconsin Integrally Synchronized Computer—a University Research Project—J. L. Asmuth, C. H. Davidson, J. B. Miller, D. S. Noble, and A. K. Scidmore. (*Commun. and Elect.*, no. 25, pp. 330–338; July, 1956.) This paper describes the functional and logical design, as well as the circuit and physical design, of the WISC (Wisconsin Integrally Synchronized Computer). The construction of the device was completed in 1955 and it is intended largely to assist in the graduate program, which function it also accomplished during its construction stage. Some of the unique logical design features include the incorporation of a synchronous instruction cycle whereby each instruction requires the same time. Although there is some loss in efficiency due to the fact that addition and subtraction are faster than multiplication and division, with the floating point operation utilized in WISC, the discrepancy in the two times is not as severe, and the advantage of having the instruction times the same for all operations more than compensates for this lack of efficiency. Because of this constant instruction time, it is possible to overlap execution cycles. Specifically, each order requires four cycles: 1) read an order; 2) locate the operands; 3) perform arithmetic; 4)deliver result. Thus, it is possible to be reading order "$n+1$" while the operands for order "n" are being located. Some logical difficulties were encountered in this procedure, such as the situation where an operand specified in order "$n+1$" might not yet be available in memory if it were also involved in order "n." However, this operand *is* available in a short memory register and can be utilized. Another situation as to specified operands might result in a conflict by which the machine would be trying to read and write in the same location during the same cycle. Such a conflict is detected by the machine and a delay cycle is automatically inserted. The machine's timing is tied to a drum on which the data are recorded, and on which the arithmetic and short memory recirculating registers are found. A three-address logic is utilized specifying the addresses of the two operands and the result. A very novel feature of the logic was the incorporation of additional circuitry to perform *automatically* floating point arithmetic. The rest of the circuitry seems to be quite conventional, utilizing vacuum tubes in flip-flop circuits at the relatively low 100-kc pulse rate. Most of the gate circuits utilize tubes, although some of them do use crystal diodes. In all, a total of 1400 tubes are used in the WISC. The paper describes a very interesting new computer which incorporates several novel features in its logical design.

Neal J. Dean

56-202

Digital Computers—General Purpose and DDA—Richard F. Walz. (*The Computer Handbook*, edited by Milton H. Aronson, The Instruments Publishing Co., Pittsburgh, Pa., pp. 27–33; 1955.) Descriptions and specifications of the Bendix G15 General Purpose Computer and the Bendix D-12 Digital Differential analyzer are presented. The G-15 is a binary, serial magnetic drum computer with storage for 2183 29-bit words. Minimum (single-precision) operation time for addition is 0.54 msec; multiplication and division, 16.7 msec. Random access time for the 20 long lines on the drum is 14.5 msec. Input-output are typewriter, paper tape and, optionally, magnetic tape, punched cards, and a graph plotter. The command structure and the break-point and "Mark Place" features are discussed. A short program is presented; the discussion of this program contains several errors. The D-12 DDA contains 60 integrators; word length is 7 decimal digits; speed is 100 or 200 iterations per second. The mode of integration may be interpolative, extrapolative, or rectangular. Input-output are typewriter, paper tape, and a graph plotter. Some typical problems solved on the DDA are discussed: solution of an integral equation, solution of a nonlinear differential equation, evaluation of an integral, and a split boundary-value problem. Though this article is presumably introductory in purpose, terms and concepts are used which are familiar only to those already acquainted with drum computers and DDA's.

D. W. Peaceman

56-203

Useful Applications of a Magnetic-Drum Computer—Stanley Frankel. (*Electrical Eng.*, vol. 75, pp. 634–639; July, 1956.) The kinds of processes general purpose digital computers can perform are described in broad terms. Then, using the Librascope LGP-30 as an example of a digital computer using a magnetic-drum storage, the functional design of a magnetic-drum computer is described. The operations that this computer can perform are discussed. This is followed by a brief section on the speed of operation of magnetic-drum computers. The paper is terminated by a general definition of the range of problems suitable for a drum computer.

H. T. Larson

56-204

USAF Computer Uses Magnetic Amplifiers—J. M. Carroll. (*Electronics*, vol. 29, pp. 138–139; July, 1956.) This article briefly describes a computer developed by Sperry Rand for the Air Force Cambridge Research Center. This computer, which uses a magnetic drum memory, is a two-address binary coded decimal machine. It operates at a master clock frequency of 660 kc. Diode logic is used throughout the machine and magnetic amplifiers are used to achieve power gain. The magnetic amplifiers utilize tape cores wound on stainless steel bobbins. Magnetic amplifiers of this type have functioned satisfactorily at pulse rates of 2.5 mc. The magnetic drum is mounted in a gas-tight helium-filled housing to prevent corrosion and rotates at 16,500 rpm. Besides the 2000 ten digit plus sign words of standard storage, the drum also contains 400 words of rapid access memory achieved by spacing four banks of read-write heads at 90 degree intervals around the drum periphery.

Norman F. Loretz

56-205

Logic Design of the RCA BIZMAC Computer—A. D. Beard, L. S. Bensky, D. L. Nettleton, and G. E. Poorte. (1956 IRE Convention Record, Part 4, pp. 81–87.) This paper gives a brief description of the Bizmac Computer which is designed for processing large amounts of alphanumeric information. Items (words) and messages (groups of items) of variable length are used to give optimum utilization of information storage and minimum instruction execution time. A brief review of the Bizmac system and the role of the computer in this system is first given. The paper then outlines the computer which has two sections of magnetic core memory making it possible to deliver two operands to the arithmetic unit simultaneously. Finally, a detailed discussion of several distinguishing features of the computer is given.

T. C. Chen

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—*The Editor*

56-206

Input and Output Devices of the RCA BIZMAC System—J. A. Brustman, K. L. Chien, and D. Flechter. (1956 IRE Convention Record, Part 4, pp. 88–93.) The various input and output devices of the BIZMAC System are described. Since all data are stored on magnetic tape, communication within the system is between each of the many tape units and the terminal devices. Data are created and entered into the system by means of a "Tapewriter," a typewriter with a paper tape punch. The tape created by the tapewriter is read by a transcriber which records the data on magnetic tape at 200 characters per second. One more step is involved in getting the data onto magnetic tape at 10,000 characters per second. A card transcriber is able to read 80 column cards at 400 cards per minute and record the data on magnetic tape. Automatic error detection in the card transcriber results in a stoppage of the process. Output devices consist of a 600 line-per-minute printer, a magnetic tape to punched tape converter, a typewriter for copying data from punched tape, and an interrogation unit. The printer is of the wheel type with a solenoid driven hammer for each of its 120 columns. The wheels turn continuously on a common shaft and character selection is accomplished by timing the pulse to the hammer by means of timing pulses on the printwheel shaft. Printed data comes from magnetic tape via a buffer store. The interrogation unit allows an item of information to be printed out on a typewriter on command at either a remote or local station.

L. S. Michels

56-207

A Small Coincident-Current Magnetic Memory—W. J. Bartik and T. H. Bonn. (IRE Trans., vol. EC-5, pp. 73–78; June, 1956.)This paper describes a small coincident-current memory used for buffer storage. Such a memory as part of the self-checking card-to-magnetic-tape converter, an auxiliary of the Univac system, is now in production. Typical advantages of a small coincident-current memory in computer input-output equipment, as well as some of the problems encountered in its application, are described. This memory affords the card-to-tape converter a great degree of flexibility, making it possible to read cards sidewise and check and edit information with a minimum of hardware and complexity. Memory cells consist of metallic-tape cores wound with multi-turn coils. The low currents required permit operation of the memory directly from the card-sensing brushes on writing and from a diode function-table on reading. The functional aspects of the memory and its associated electrical circuitry are described. Information concerning the physical nature of the memory, specifications of the cores, and some of the tests performed in their inspection is aslo presented.

Courtesy of Proc. IRE

56-208

A Magnetic Drum Extension to the Gamma 3 Computer—P. L. Dreyfus, H. G. Feissel, and B. M. Leclerc. (1956 IRE Convention Record, Part 4, pp. 105–108.) The paper describes a combined magnetic drum and high speed (magneto-strictive delay line) storage unit intended to convert the Gamma 3 of the Compagnie des machines Bull in Paris into an essentially internally programmed drum computer. Drum capacity is nearly 400,000 bits, divided into 64 tracks of eight blocks each. High-speed storage consists of 64 magneto-strictive delay lines storing 48 bits each: a group of 16 lines is equivalent to one block on the drum. During a transfer from drum to one block of 16 lines the 48 remaining lines can be used by the machine thus enabling computation to proceed during transfers. Arithmetic manipulation of instructions and automatic transfers to and from subroutines have been made possible. Some details are given about technical aspects of delay line and head construction. The synchronization scheme of drum, master clock, and delay lines is discussed briefly. No data are present on drum dimensions and packing density. Programming for the computer is not discussed.

B. J. Loopstra

56-209

Burroughs G-101 High Speed Printer—E. M. DiGiulio. (1956 IRE Convention Record, part 4, pp. 94–100.) Those well-versed in the computer art will find this paper a clear description of the technical features of the printer, a product of the Control Instrument Company, subsidiary of Burroughs. The printer produces 900 forty-eight character lines per minute from punched cards. Each character is formed by selected wire ends from a 5×7 matrix striking the paper through carbon. Each wire is actuated by common power shaft through a magnet controlled trigger mechanism. The 35 magnets for each character are controlled through a diode matrix by 13 relays, one for each of the 12 holes in a card column and one for zero suppression. The relays are set up by a thyratron which senses the card holes. A gas tube counter and core shift register storage to be added are also described. A future bill feed and punch are also mentioned. The first unit was delivered in February, 1956.

M. M. Astrahan

621-52 56-210

A Three-Dimensional Machine-Tool Control System—(*Electronic Eng.*, vol. 28, pp. 204–207; May, 1956.) Programming instructions taken from design drawings are worked out by an independent digital computer and recorded on magnetic tape which is used in a control unit to operate the machine tool. For measurement purposes an optical diffraction grating system is associated with each plane of the tool and in combination with a photosensitive detector produces a pulse train which is locked to the command pulse train through a servomechanism.

Courtesy of Proc. IRE and *Wireless Engineer*

56-211

An Electronic Machine for Statistical Particle Analysis—H. N. Coates. (*Proc. IEE*, Part B, vol. 103, pp. 479–484; July, 1956.) In physical research it is sometimes necessary to scan photographs of a field of particles photo-electrically to gain information about particle shape and size. Author's summary: A system is described for associating and collecting the intercepts of individual particles in a particle scanning system, where the information is presented as a function of the scanning voltages. A series of stores is used to segregate the intercepts, each store having its own memory system and provision for re-use on completion of the scanning of the particle with which it is associated; the stores can thus be used many times during a single frame scan. A method of adding the intercepts of each particle to obtain a measure of the area of the particle is described, but this must be regarded as only one of the possibilities of extracting information from the series of intercepts collected.

D. E. Hart

56-212

A Transducer for Digital Data-Transmission Systems—R. H. Barker. (*Proc. IEE*, Part B, vol. 103, pp. 42–51; January, 1956.) Author's summary: Accurate information such as may be required for weapon control may best be transmitted over long-distance telegraph or voice communication circuits by using some form of digital representation or pulse code modulation. The paper describes a method by which the position of a scale attached to a datum shaft may be "read" photoelectrically as a binary number in much the same way as the scale of a surveying instrument is read in degrees and minutes. Data-transducers have been constructed to represent the angular position of a shaft as a 14-digit binary number, that is to an accuracy of rather better than one minute of arc. Special precautions have been taken in the design of the scale to prevent gross errors due to movement of the scale while it is being read. Such errors as do occur are examined in detail, since in some data-transmission applications they may not be sufficiently serious to justify the more complex equipment required for their complete elimination.

D. E. Hart

56-213

Wind-Tunnel Data Reduction Using Paper-Tape Storage Media—William R. Hoover, John J. Wedel, and Joseph R. Bruman. (*J. Assoc. Comp. Mach.*, vol. 3, pp. 101–109; April, 1956.) Twenty-four components of force, torque position, and pressure are accumulated on punched paper tape together with semiautomatically punched computer commands and handset tag data. The tape can then be printed out on a tab sheet (Flexowriter) or plotted for inspection by tunnel personnel. The tape is then fed to an Electrodata 36-102 with a modified input-output system which can reduce one point of data, including all rearrangement of data in approximately 20 seconds. This means that daily data reduction is now possible.

W. A. Farrand

681.142:519.272.:534.6 56-214

Measurement of Correlation Coefficient—S. G. Gershman and E. L. Feinberg. (*Akust. Zh.*, vol. 1, pp. 326–338; October /December, 1955.) The determination of the correlation coefficient of af noise is based on the measurement of the coincidences of sign of rectangular pulses triggered by the incoming signals. The instrument is described in detail and the theory of operation is given.

Courtesy of Proc. IRE and *Wireless Engineer*

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—The Editor

681.142:621.374.3 56-215

An Electrostatic Pulse Generator—W. Woods-Hill. (*Electronic Eng.*, vol. 28, pp. 122–123; March, 1956.) Pulse patterns required in electronic computers are generated by presenting a probe feeding a tuned amplifier to a suitably figured track on an insulated rotating drum carrying a rf voltage.

Courtesy of PROC. IRE and *Wireless Engineer*

UTILIZATION OF DIGITAL EQUIPMENT

681.142 56-216

The Design, Construction and Applications of Electronic Digital Computers—E. Grundy and H. McG. Ross. (*Trans S. Afr. IEE*, vol. 46, Part 10, pp. 261–294; October, 1955.) A survey of the whole field, with a comprehensive bibliography; a wide range of actual and projected applications in science and industry is discussed, including process control and data analysis.

Courtesy of PROC. IRE and *Wireless Engineer*

56-217

EASIAC, A Pseudo-Computer—Robert Perkins. (*J. Assoc. Comp. Mach.*, vol. 3, pp. 65–72; April, 1956.) Students in a two-week summer course in computers at the University of Michigan are introduced to the principles of coding by means of a translation-interpretation program which simplifies the use of the MIDAC computer. In conjunction with this program, the MIDAC becomes, in effect, a smaller, slower, less complicated and less versatile machine called EASIAC. The article describes the method of coding for EASIAC; the nature and form of the instruction codes are discussed and illustrated. Of particular interest is an example of the printout after the automatic detection of a programming mistake. Four kinds of information are tabulated to serve as an aid in determining the location and nature of the mistake. An appendix describes concisely the twenty-five EASIAC operations and lists the mneonic alphabetic code by which each is specified.

S. H. Lewis

56-218

Phase Calculations for Nuclear Scattering on the Pilot ACE—H. H. Robertson. (*Proc. Cam. Phil. Soc.*, Part 3, vol. 52, pp. 538–545; July, 1956.) The integro-differential equations appearing in the theory of nuclear scattering were reduced to simultaneous algebraic equations by the use of finite-difference approximations. The whole calculation comprises several stages: the calculation of the kernels, the derivation of the coefficients in the simultaneous equations, the solution of these equations to give the wave function, and the evaluation of the phase. All these were performed on the Pilot ACE, and the paper describes briefly the mathematical theory and the plan of the computations. Although several scattering processes have been investigated, only one very simple example is given in the paper.

Stanley Gill

56-219

A Numerical Calculation of the General Circulation of the Atmosphere—(*Nature*, vol. 178, p. 129; July 21, 1956.) This one-page article is in part a review of a paper in the April issue of the *Quarterly Journal of the Royal Meteorological Society* by N. A. Phillips, Institute for Advanced Study, which describes an experiment in the numerical calculation of atmosphere changes allowing for friction and nonadiabatic heating. The calculation starts with the atmosphere at rest and of uniform temperature, then proceeds to steady state at 130 days. The effect of perturbations is then studied.

D. E. Hart

56-220

Approximating Functions for Digital Computers—L. R. Landgon. (*Industrial Math.*, vol. 6, pp. 79–100; 1955.) In this paper the author uses a modified Taylor expansion due to Hummel and Seebeck and appearing in the American Mathematical Monthly, April, 1949, to derive some very good approximating functions for the commonly encountered functions e^x, $\sin x$, $\cos x$, $\tan x$, x^p(p real). To approximate e^x, $-\pi \leq x \leq \pi$, with an error of one unit in the ninth significant digit, for example, he obtains

$$e^x = \frac{\sum_0^3 a_{2k}\left(\frac{x}{3}\right)^{2k} + \frac{x}{3}\sum_0^3 b_{2k}\left(\frac{x}{3}\right)^{2k}}{\sum_0^3 a_{2k}\left(\frac{x}{3}\right)^{2k} - \frac{x}{3}\sum_0^3 b_{2k}\left(\frac{x}{3}\right)^{2k}}.$$

The coefficients a_{2k}, b_{2k} cannot be generated easily but must be stored. This is a no handicap if a subroutine is being written for a digital computer. It appears to suffer from the disadvantage that for greater accuracy one must use a formula whose coefficients are different from those given above and, hence, these coefficients must again be stored. The author also obtains approximations to Arc tan x, Arc sin x, $\log_e x$, and the error function using Chebyshev polynomials. There are some printing errors as well as some numerical errors in this paper. The most serious of these are 1) on p. 88, (8.1), the number C_7 should be negative instead of positive, and 2) on p. 87, line 22, the expression for sin x should be

$$\sin x = 0.9999\ 99031x - 0.16666\ 53749x^3 + 0.00832\ 86830x^5 - 0.000\,1922123x^7 + R.$$

S. D. Conte

BOOK REVIEWS

56-221

Electronic Computers and Management Control—George Kozmetsky and Paul Kircher. (McGraw-Hill Book Co., New York, N.Y., 296 pp., 1956.) Written in nontechnical language for business executives, this book explains how computers operate, shows how they can be applied to such functions as accounting, production scheduling, or cost control, and gives information on input, processing, storage, control, and output. It deals also with the basic concepts of scientific methods for analyzing business data for management planning and control and with the tools of the analyst—linear programming, calculus of variations, information theory, stochastic models, etc., An appendix gives specific details of currently available commercial equipment.

Courtesy of *Electrical Eng.*

56-222

Automation, Friend or Foe?—R. H. Macmillan. (Cambridge University Press, New York, 100 pp. +viii, illus.; 1956.) The author presents some historical aspects of automatic control and illustrates these aspects with familiar examples. His experience is primarily British and so are most of his illustrations of recent advances in the field. In the author's opinion automation need not lead to unemployment but should lead to a general upgrading of skills and an increase in leisure time for the working man. On topics familiar to the reviewer some inaccuracies are noted. For example, the ENIAC can perform 400 multiplications of two ten-figure numbers per second instead of 40 as stated on page 66. On the same page, the statement that on the EDSAC "addition is six times as fast as with ENIAC" is erroneous; in fact, the EDVAC is effectively at least five times slower than the ENIAC in addition or subtraction operations. Similarly, the statement on the following page that the Whirlwind computer "will perform 200,000 additions or 25,000 multiplications in a second" is inaccurate. Actually, it can perform 25,000 additions of sixteen binary bit numbers per second. In summing up, according to the author: Automation will make possible greater dispersion of population, automatic devices have very definite limitations but their further use may make a radical change in the economy, one need not be alarmed at the social changes that will follow automation. He goes, on to state that whether or not one agrees with the last statement there can be no doubt that in this highly competitive world any method of manufacture that is more efficient must be used whenever possible in order for a country, such as Britain, to retain or expand its export trade. At the conclusion, the author briefly analyzes further reading which is available on automation.

Harry D. Huskey

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